# In Situ Delay-Slack Monitor for High-Performance Processors Using An All-Digital Self-Calibrating 5ps Resolution Time-to-Digital Converter

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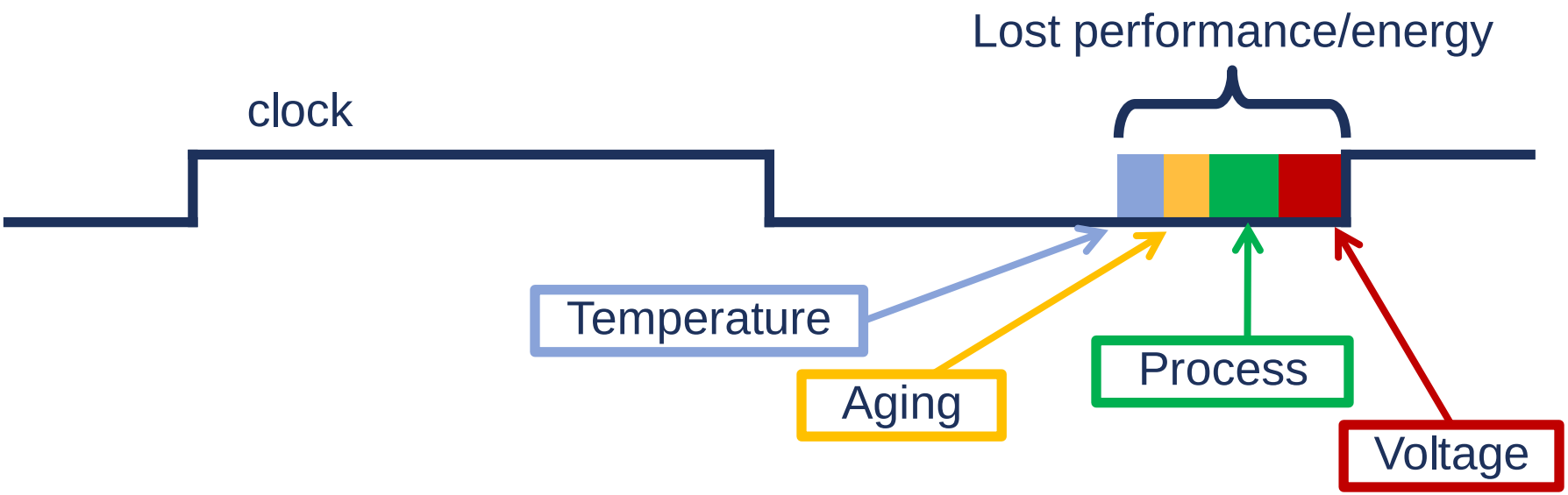
# Timing Margins

Margins for uncertainty:

- Process Variation
- Temperature Variation
- Voltage Variation
- Aging Effects

Associated Costs:

- Lost performance
- Lost energy
- Tester time (tradeoff)



# Timing Margin Reduction

| | | Detect and Correct (e.g. Razor) |
|---|---|---|
| Margin Reduced | Global Variation | Yes |
| | Local Variation | Yes |
| | Fast Variation | Yes |
| | Introduced | None |
| Cost | Area | Large |
| | Invasiveness | Large |
| | Tester Time | Small |

# Timing Margin Reduction

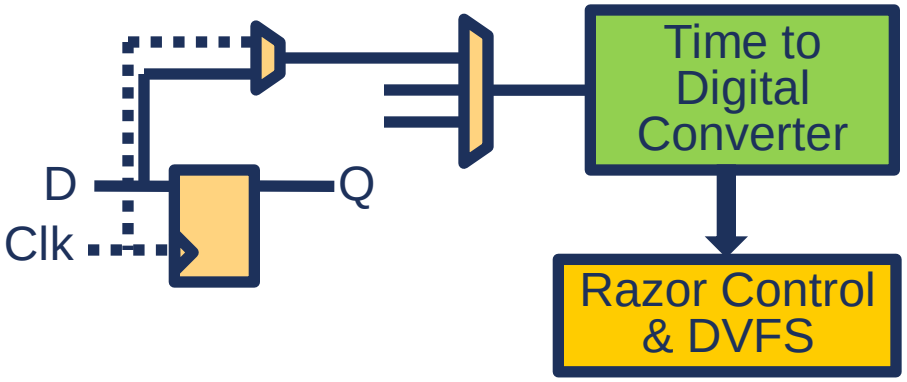
| | | Detect and Correct (e.g. Razor) | Prediction via Canaries and Sensors |
|---|---|---|---|
| **Margin Reduced** | **Global Variation** | Yes | Yes |
| | **Local Variation** | Yes | No |
| | **Fast Variation** | Yes | No |
| | **Introduced** | None | Sensor Tracking<br>Sensor Variation |
| **Cost** | **Area** | Large | Small |
| | **Invasiveness** | Large | Small |
| | **Tester Time** | Small | Typically Large |

# Timing Margin Reduction

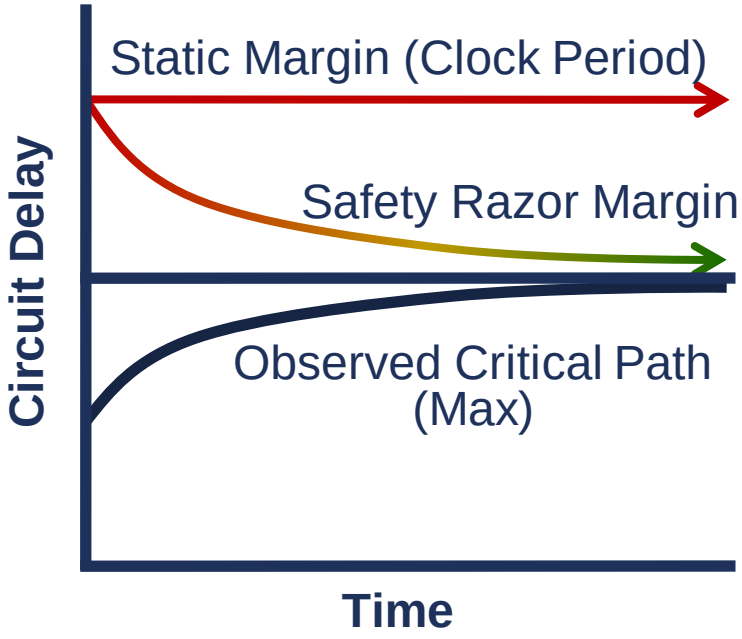
| | | Detect and Correct (e.g. Razor) | Prediction via Canaries and Sensors | Delay Slack Monitoring (This Work) |
|---|---|---|---|---|
| **Margin Reduced** | **Global Variation** | Yes | Yes | Yes |
| | **Local Variation** | Yes | No | Yes |
| | **Fast Variation** | Yes | No | No |
| | **Introduced** | None | Sensor Tracking<br>Sensor Variation | TDC Accuracy |
| **Cost** | **Area** | Large | Small | Small |
| | **Invasiveness** | Large | Small | Small |
| | **Tester Time** | Small | Typically Large | Small |

# Proposed Application - Safety Razor

- Accurately measure delay slack at each critical flop
  - Subtract:
    - Data Delay
    - Clock Delay

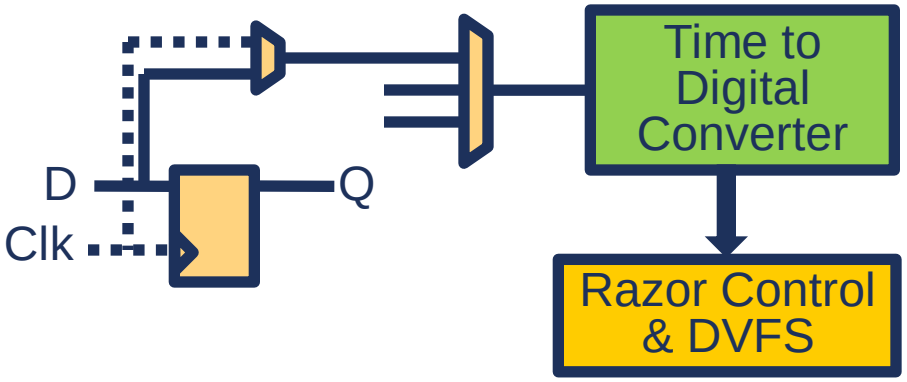


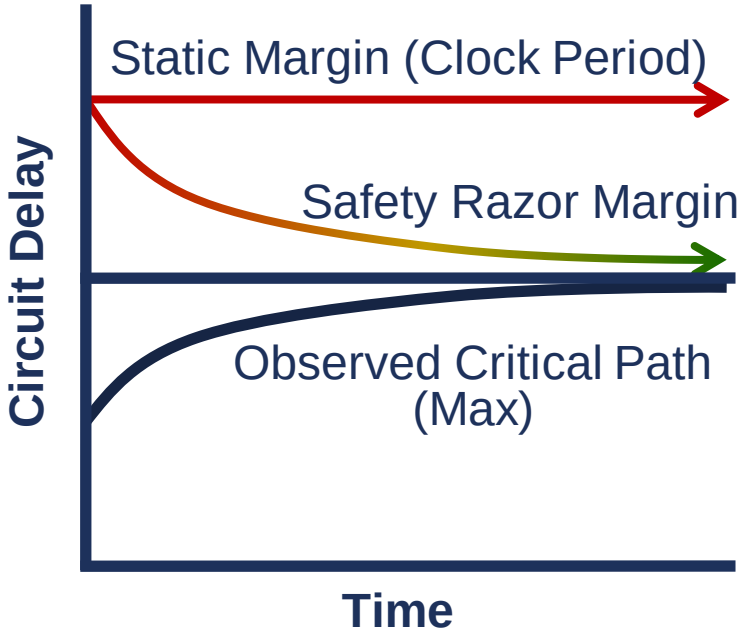

- Applications:
  - Known stable code bases
  - Large number of crit. flops



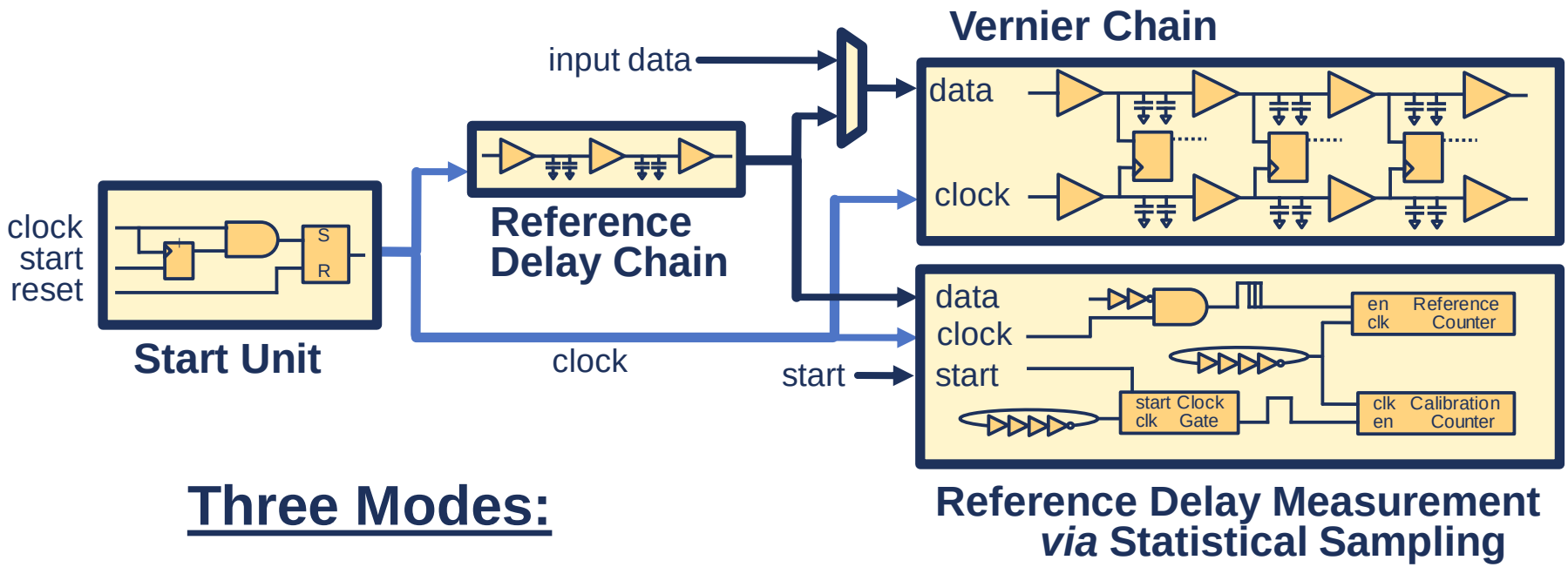
# Proposed Application - Safety Razor

- Need:
  - High-speed, high accuracy time-to-digital converter
  - Low tester time
- This work:
  - 5ps measurement steps
  - 150ps measurement window, movable
  - *In-situ* self calibration
    - Uses bus clock for reference
    - No tester time
    - No CPU downtime



# TDC Architecture

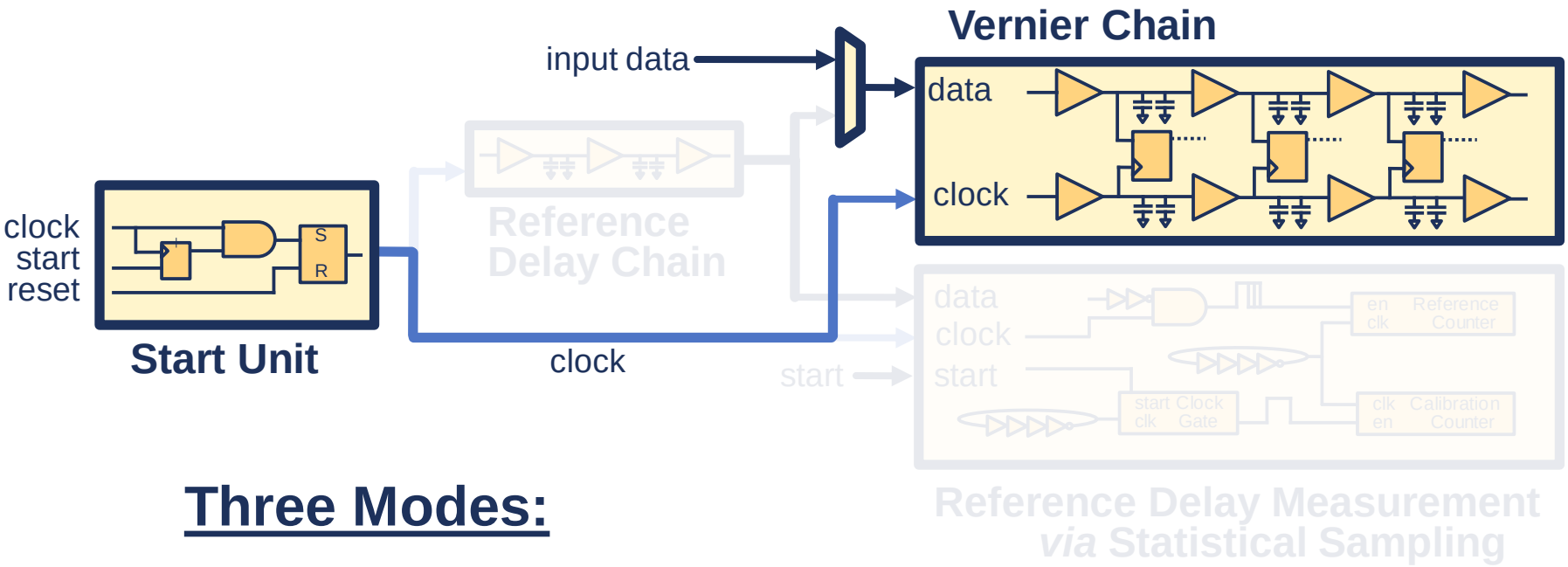



## Three Modes:

- Normal Operation
- RDC Calibration
- VC Calibration

# TDC Architecture

## Normal Operation

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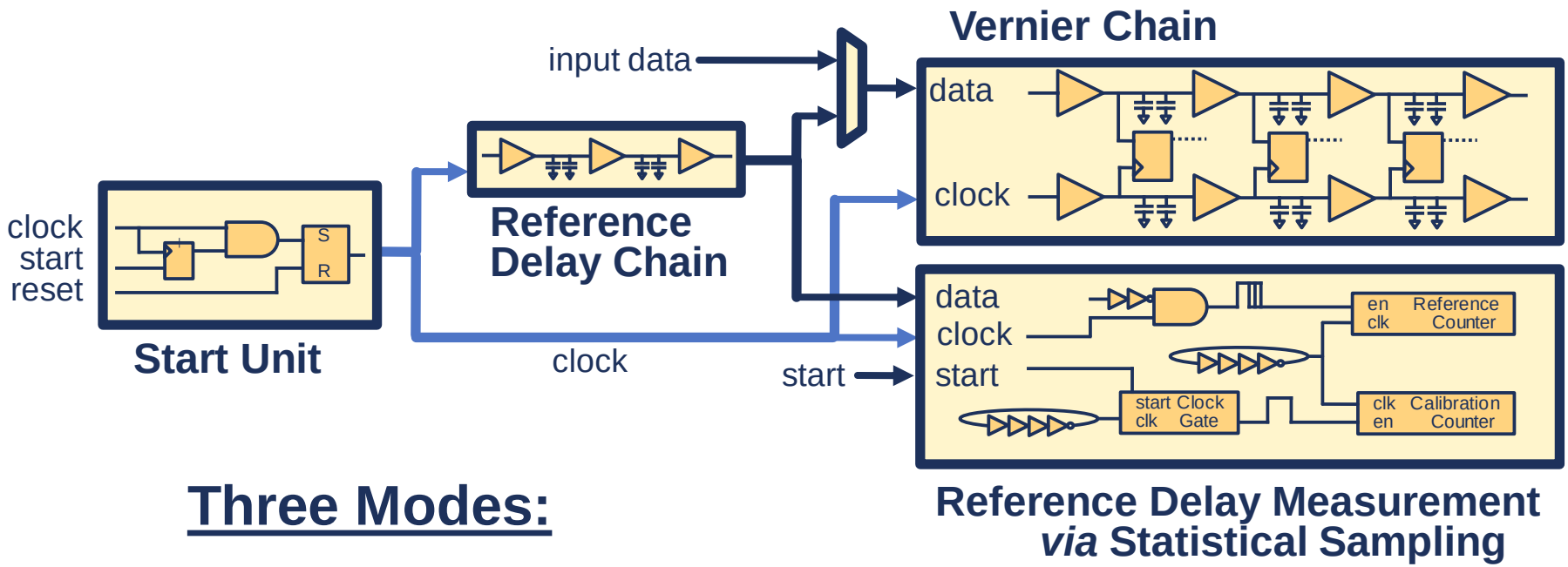


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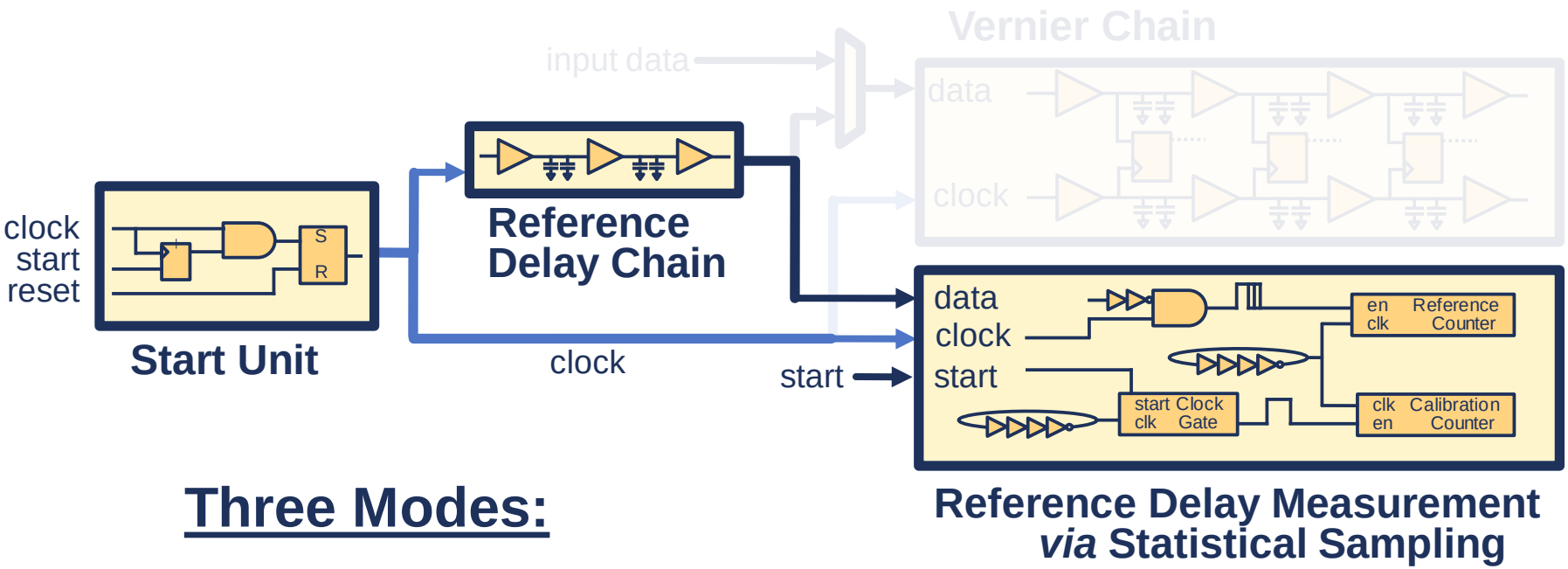
# TDC Architecture

## Reference Delay Calibration

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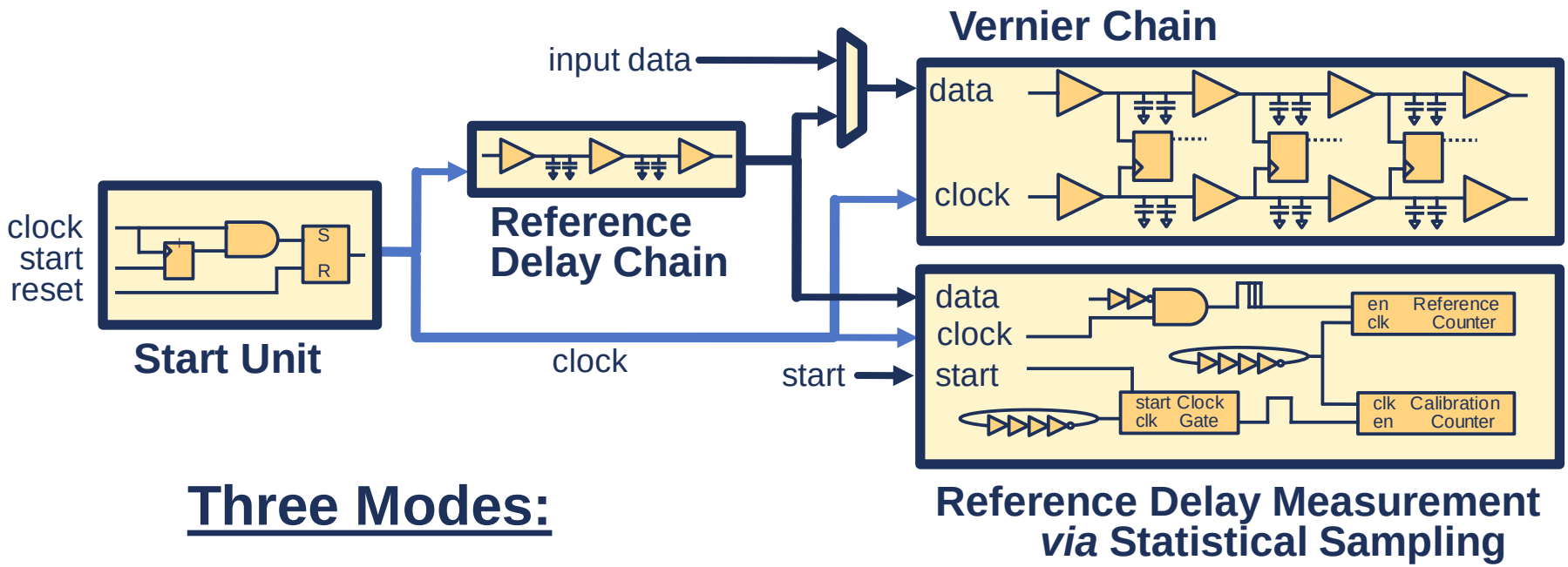


## Three Modes:

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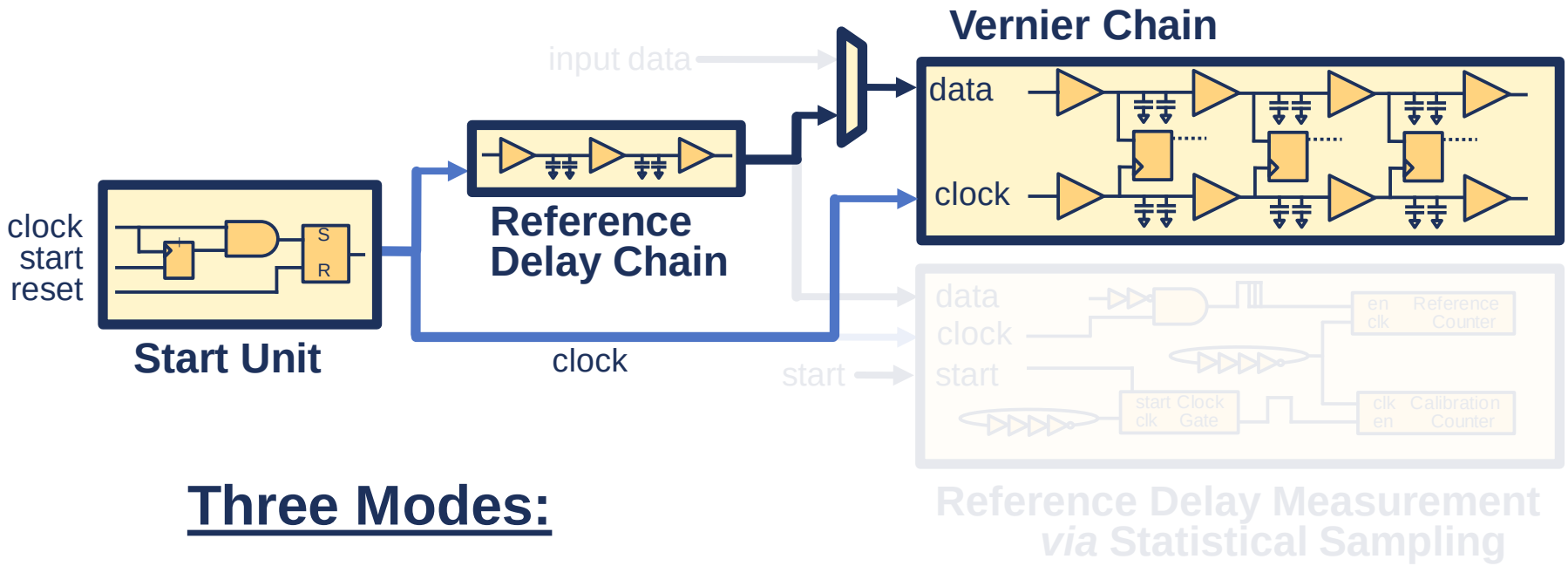
# TDC Architecture

## Vernier Chain Calibration

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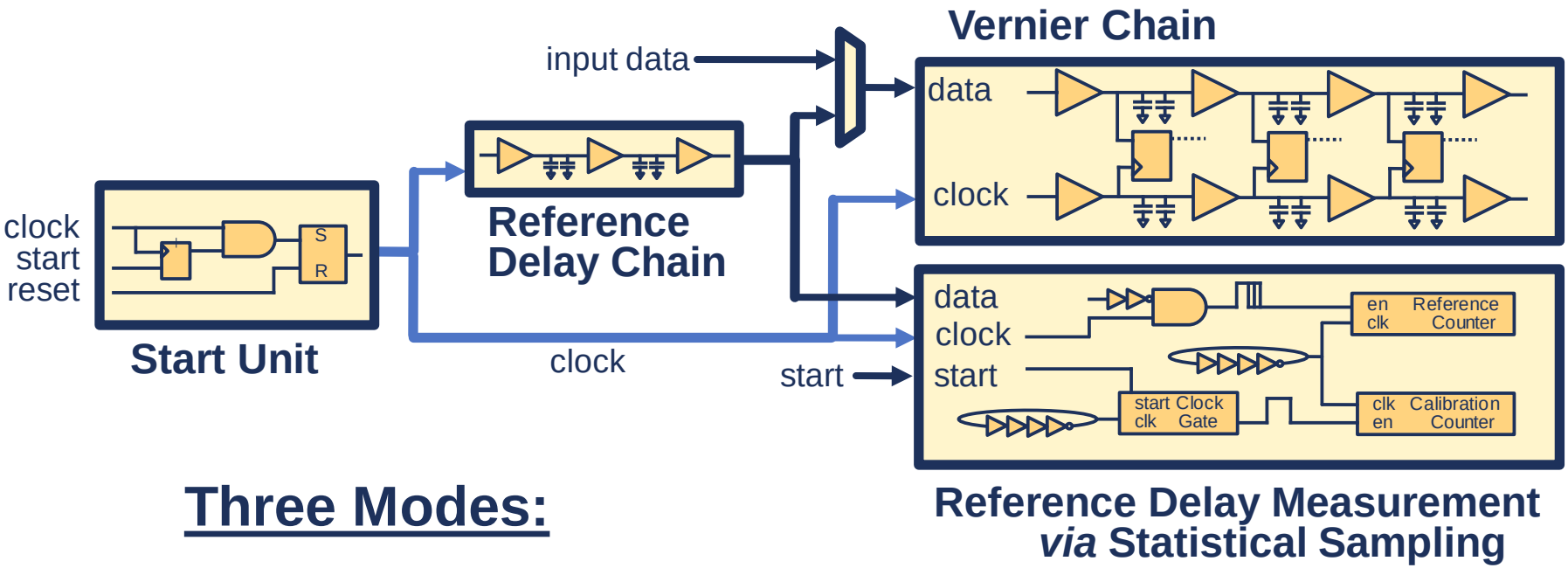


## Three Modes:

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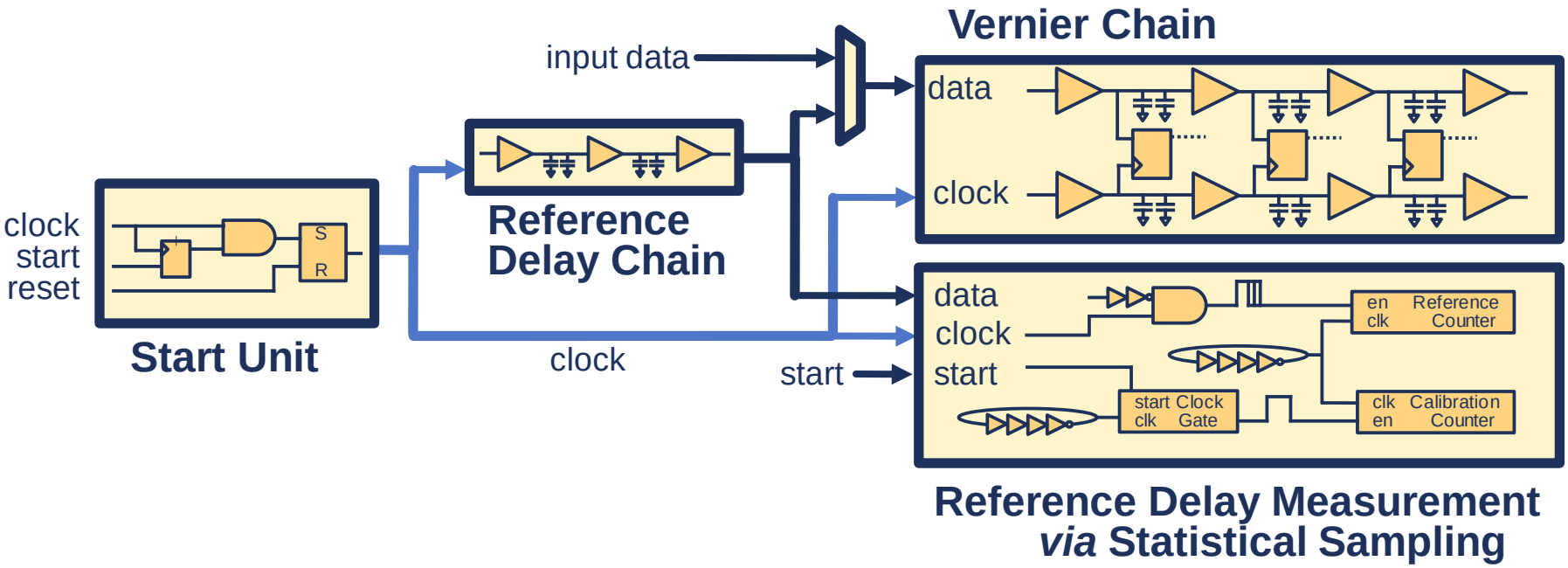
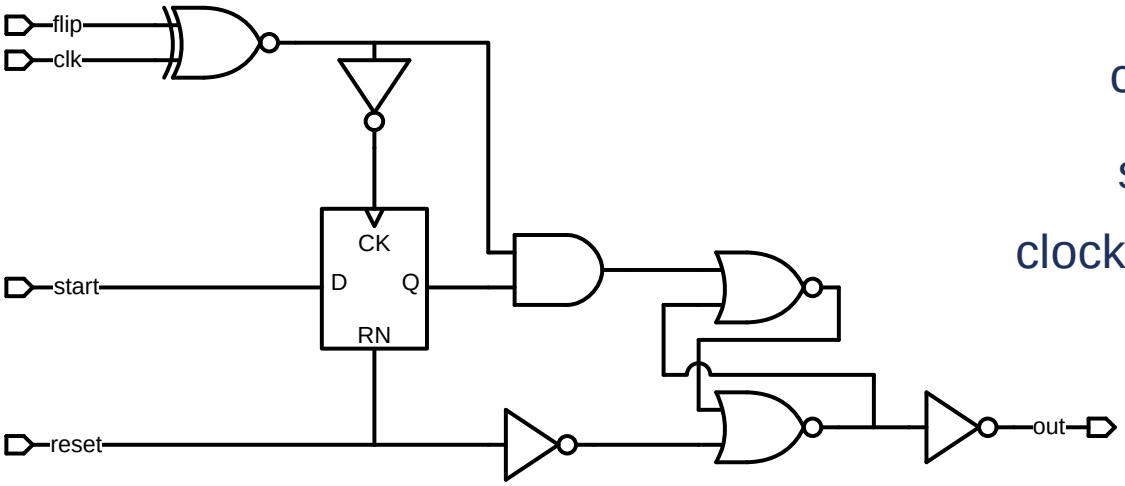
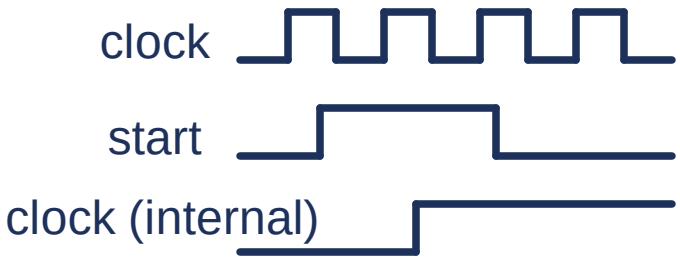
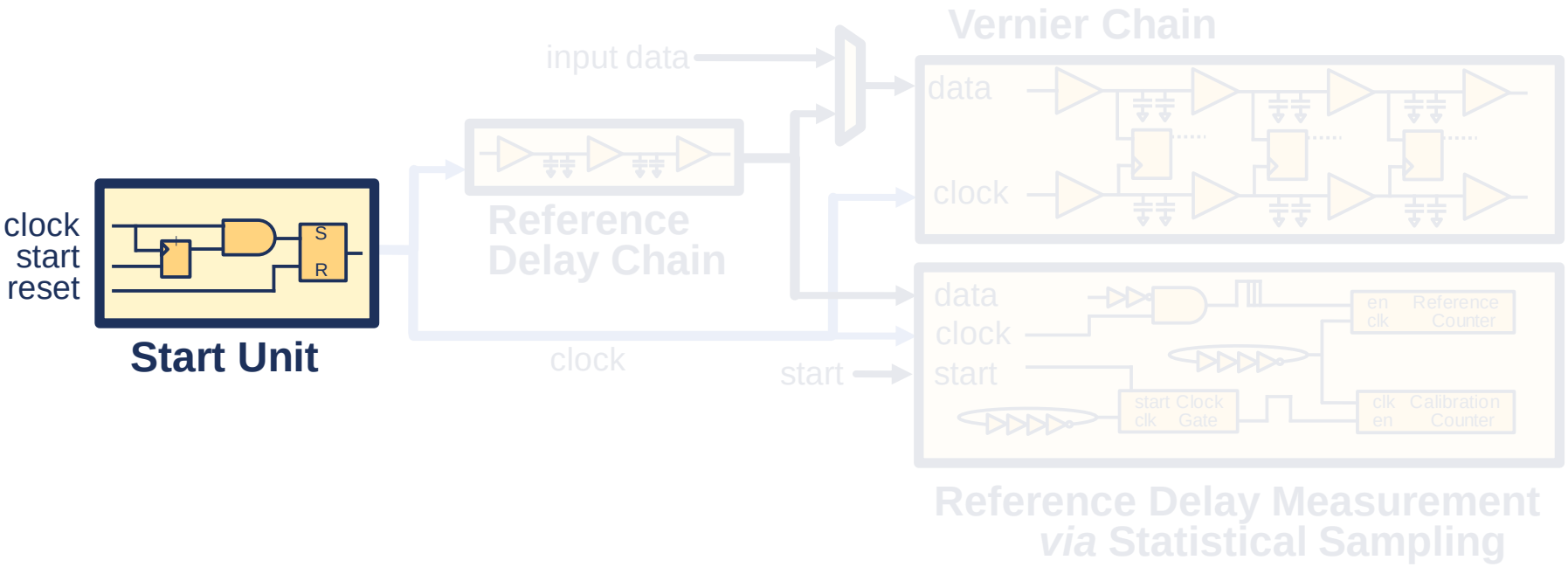
# TDC Components



# TDC Start Unit



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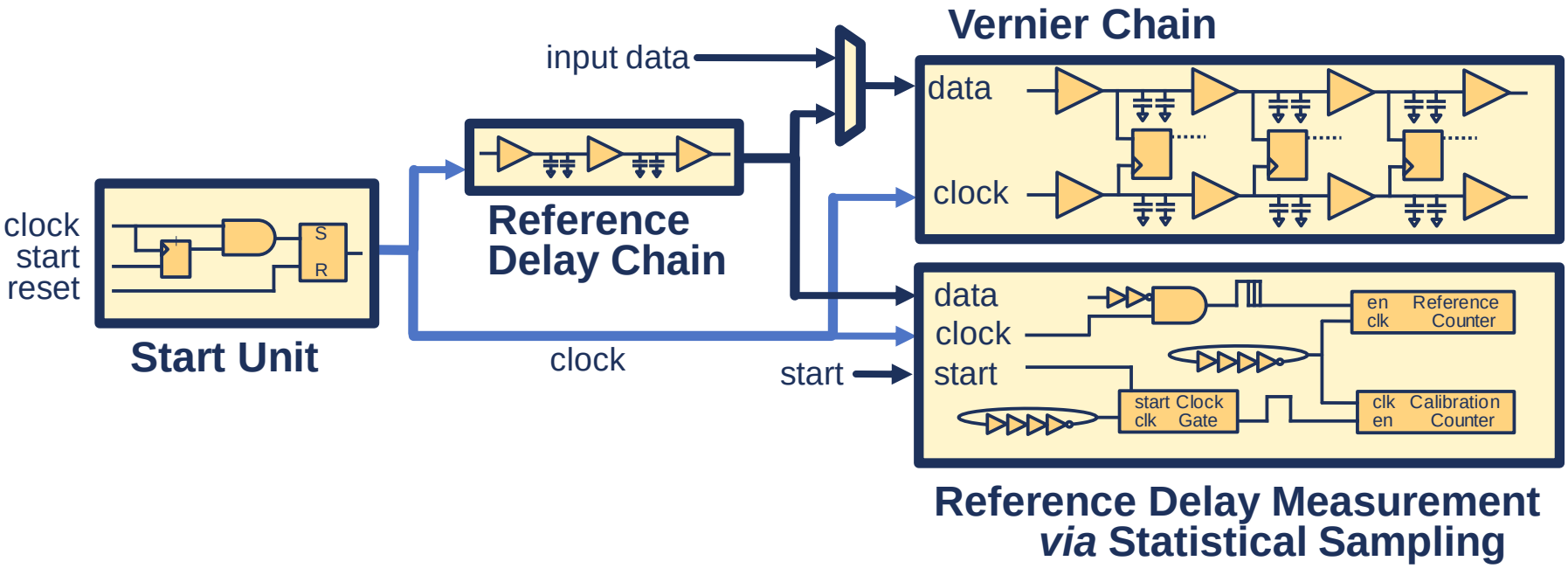
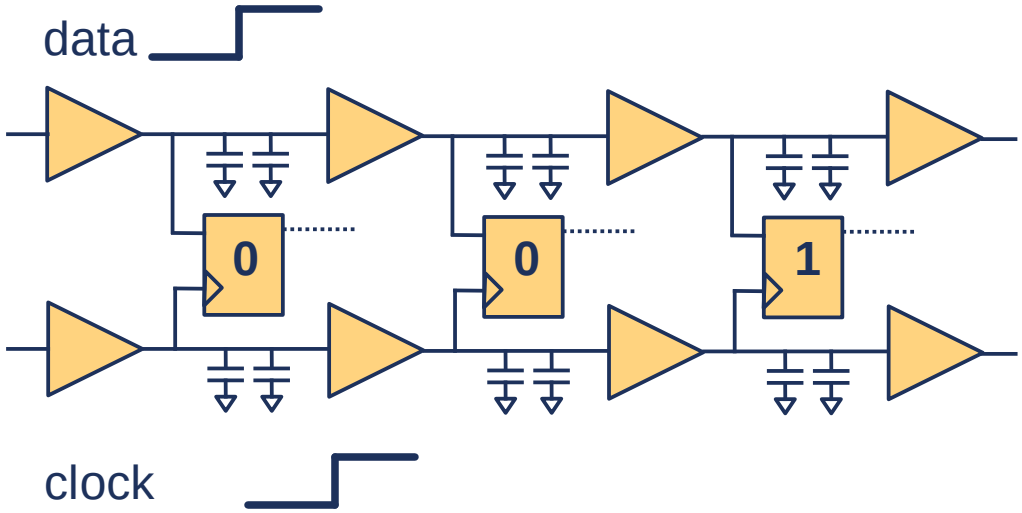
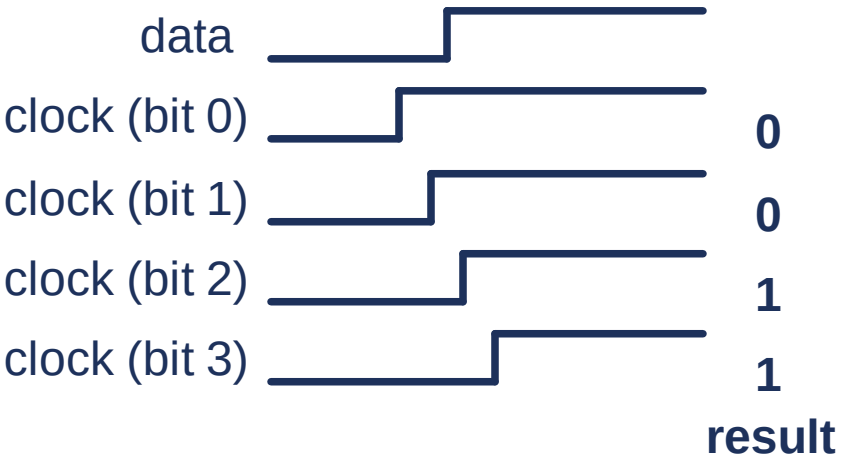
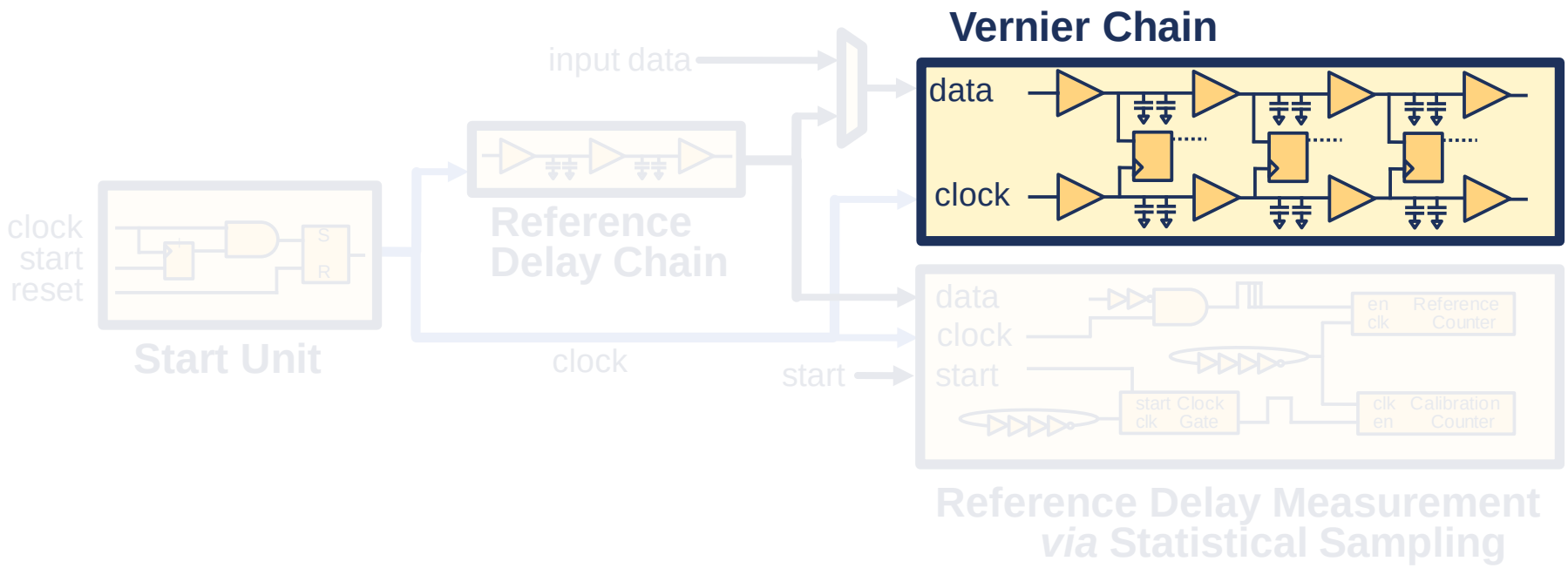


# TDC Vernier Chain



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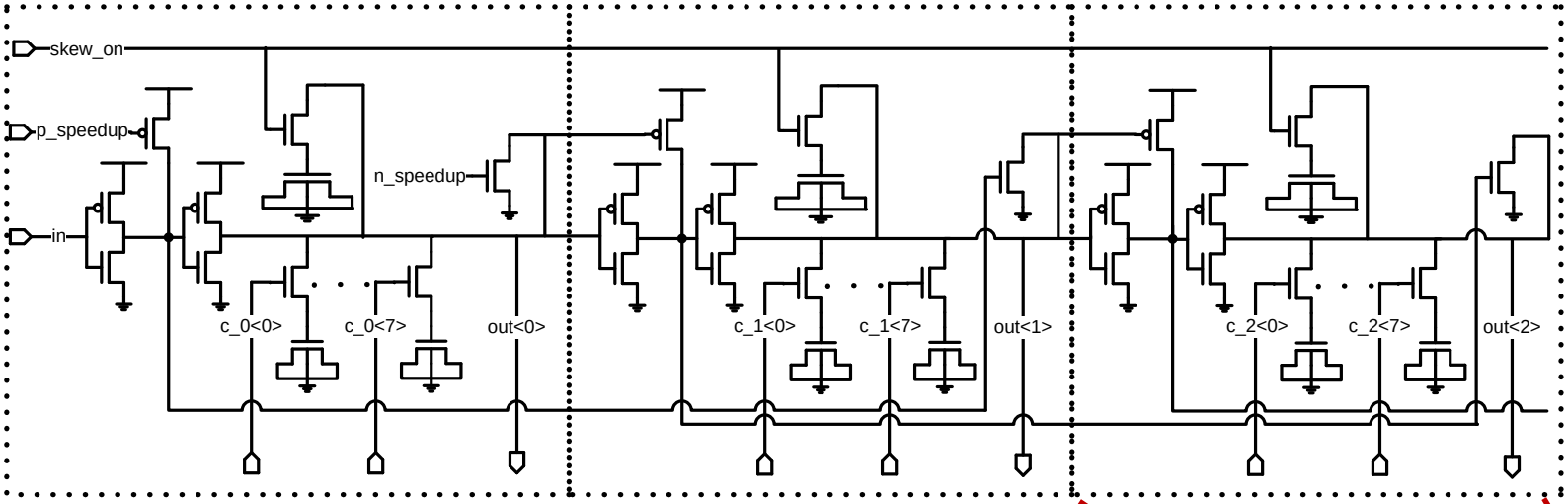


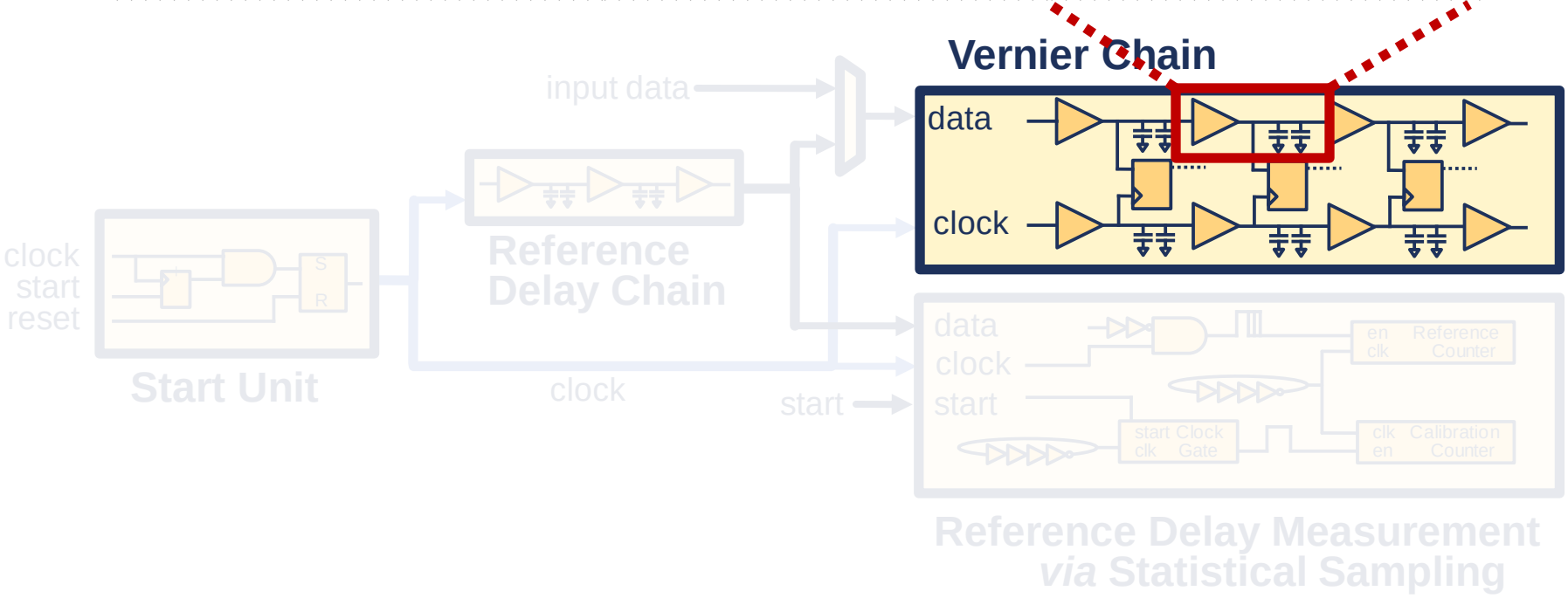

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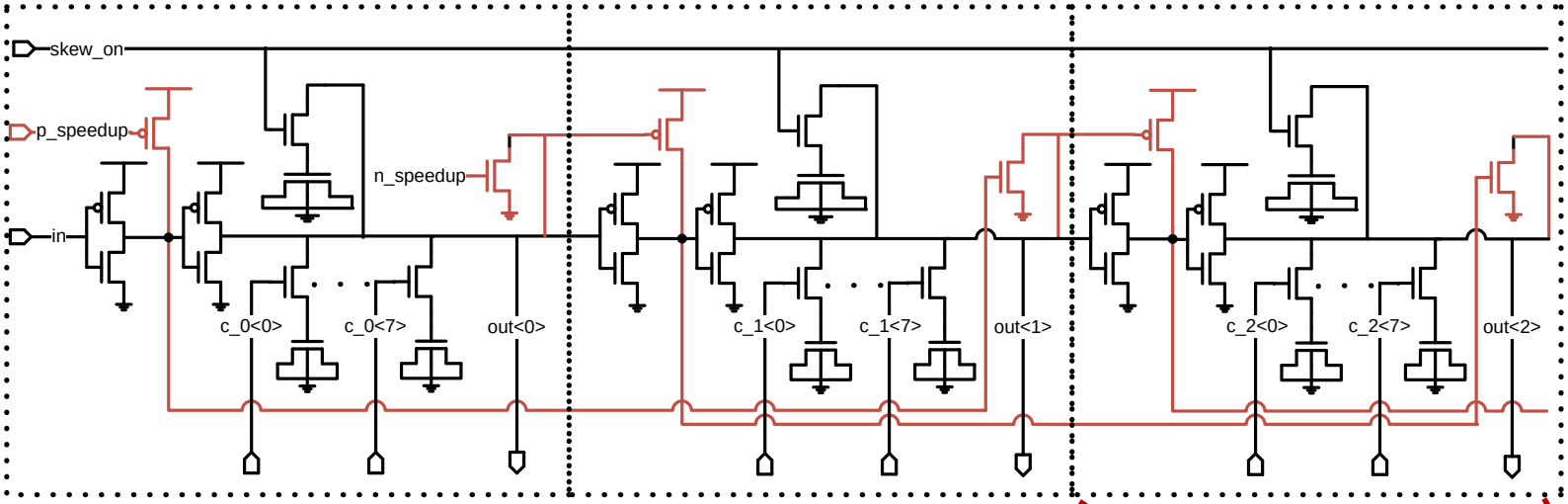


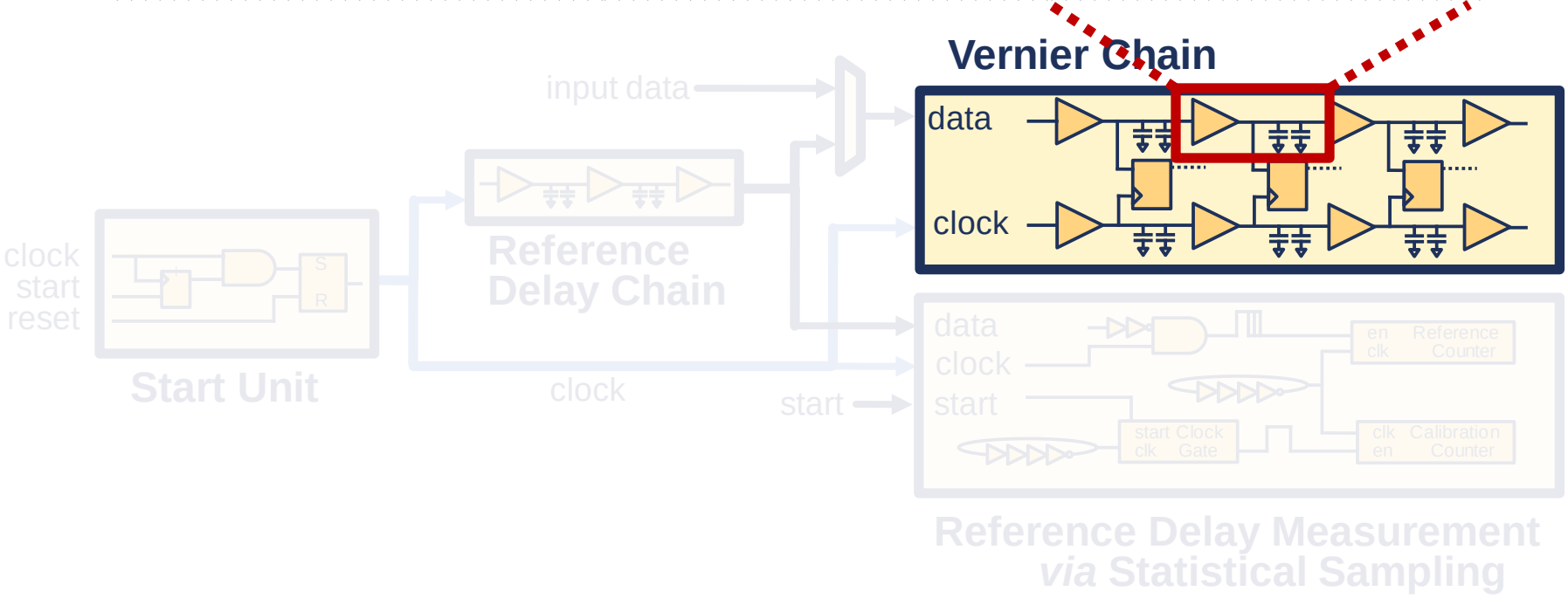

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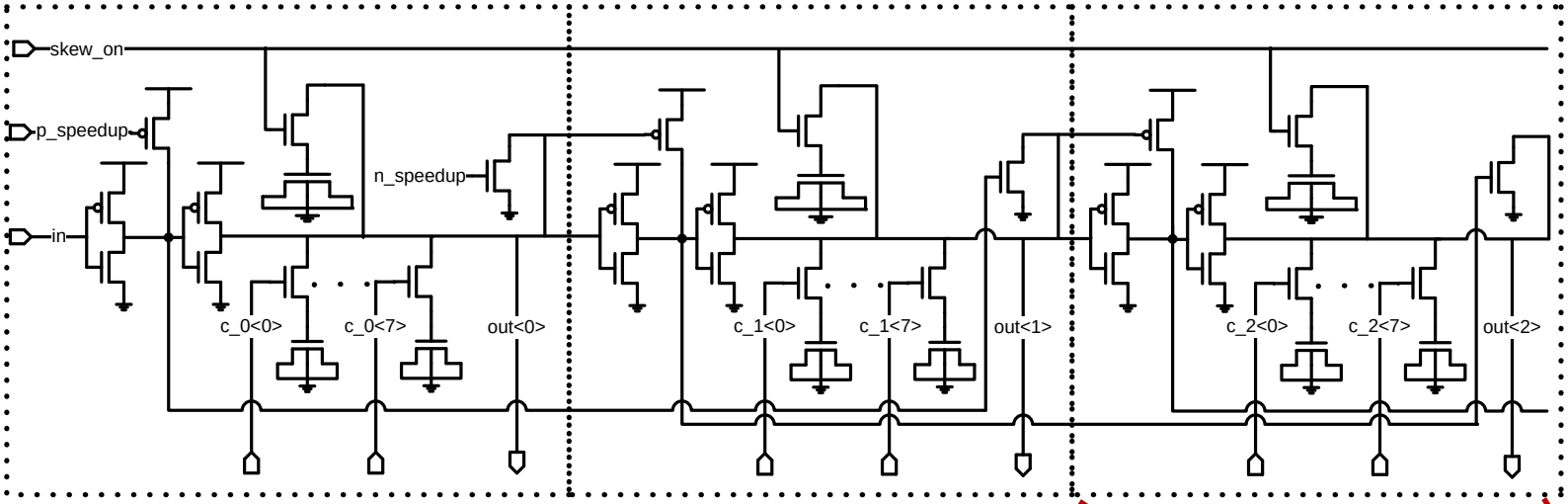
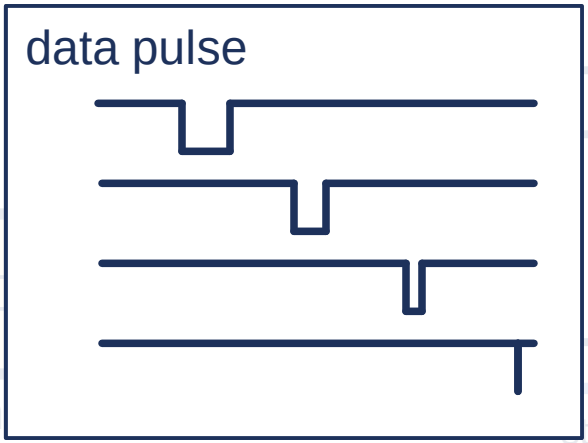
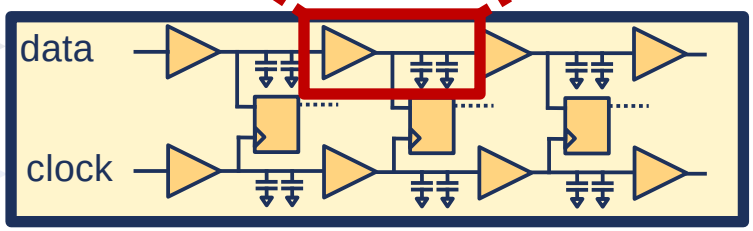




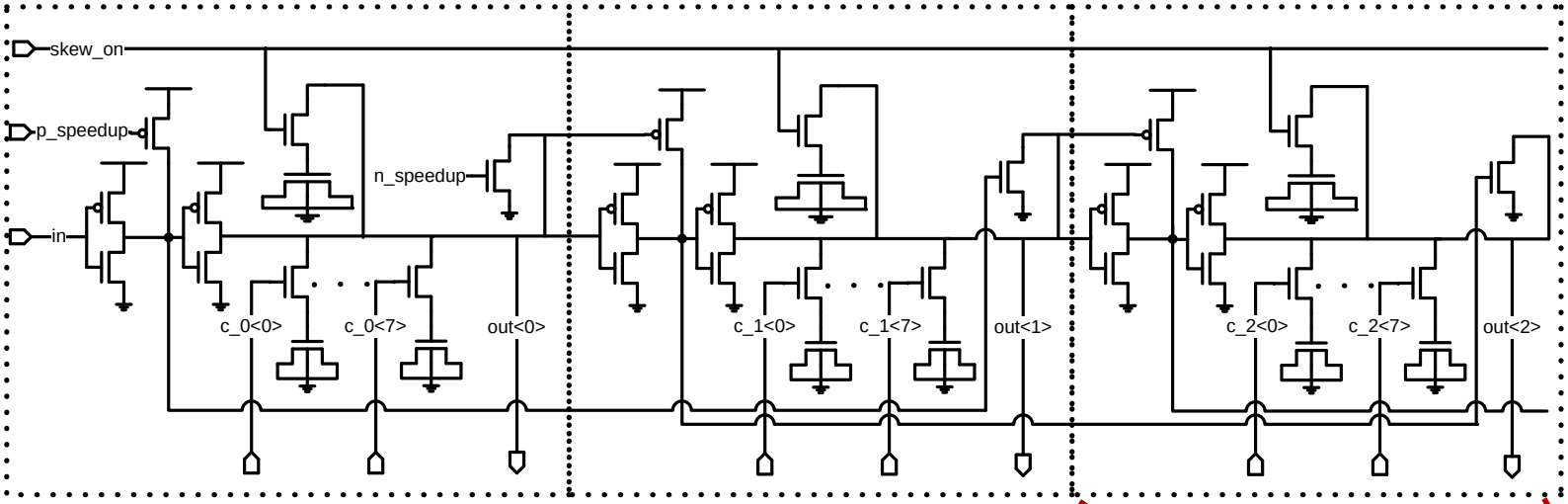


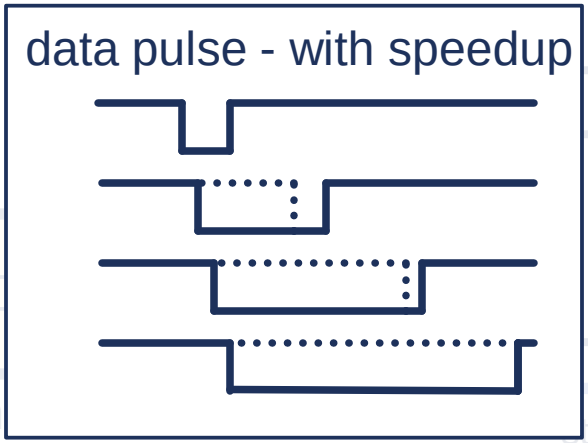
Start Un

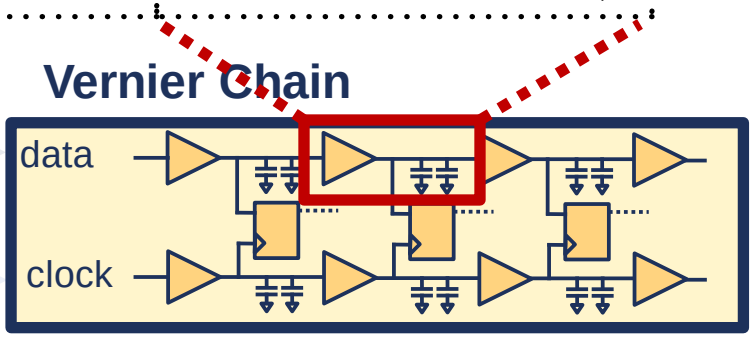



Reference Delay Measurement *via* Statistical Sampling

# TDC Vernier Chain







Start Un




Reference Delay Measurement *via* Statistical Sampling

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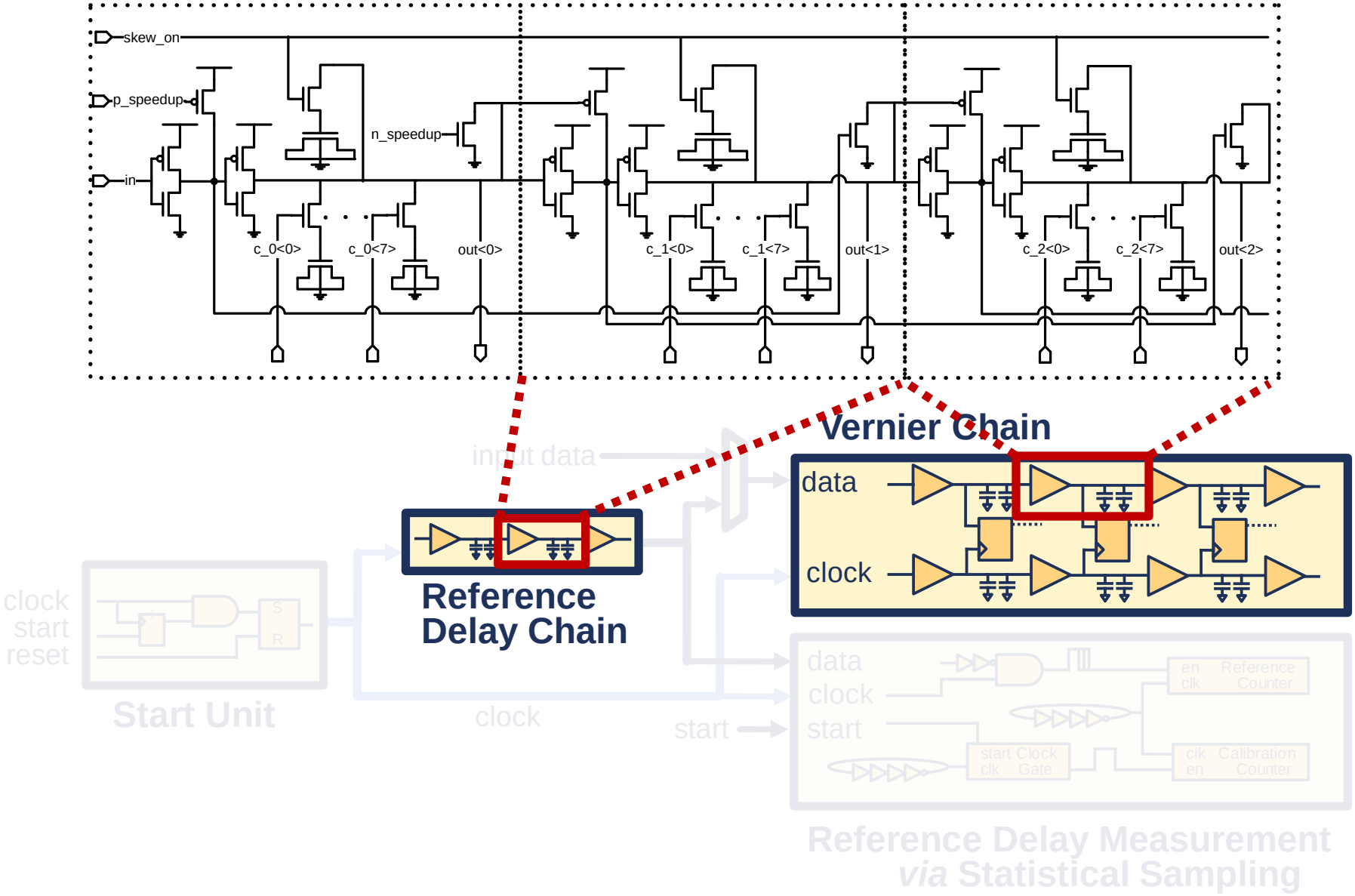

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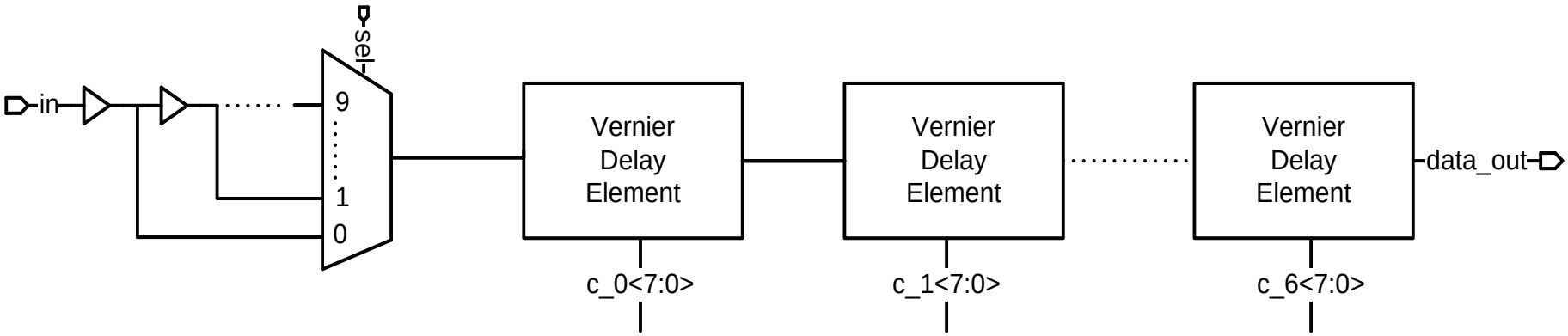
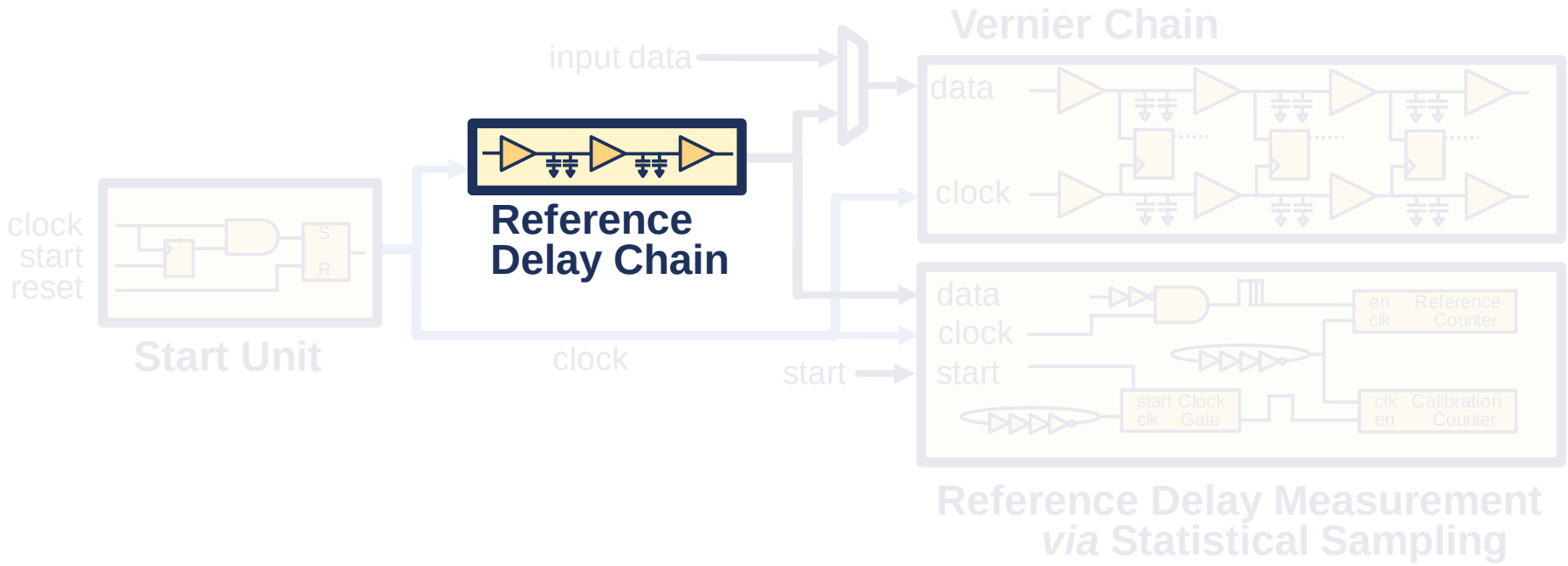
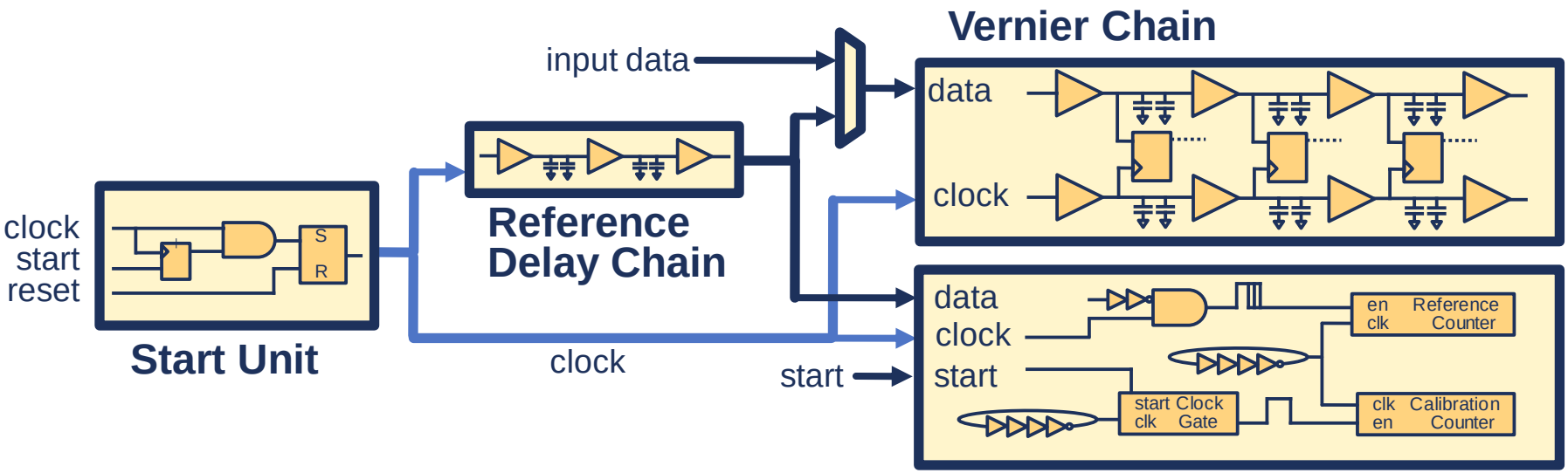


# TDC Calibration

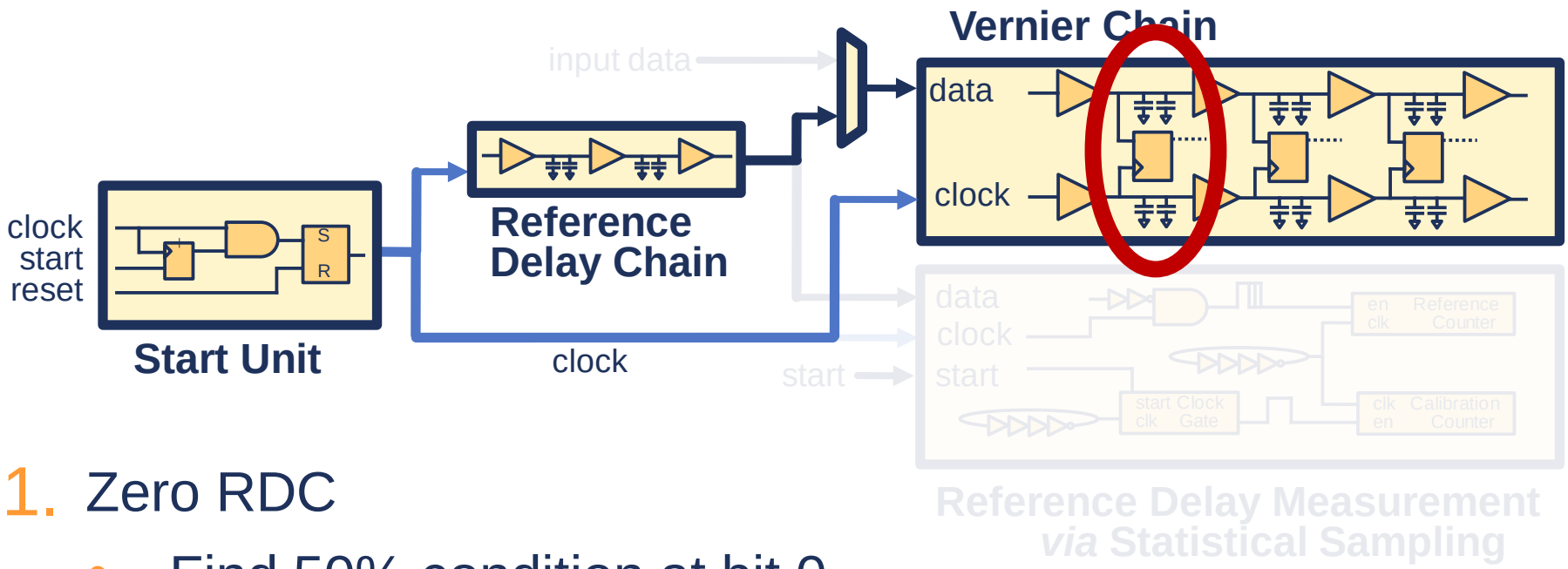



Reference Delay Measurement *via* Statistical Sampling

Use RDC to calibrate VC

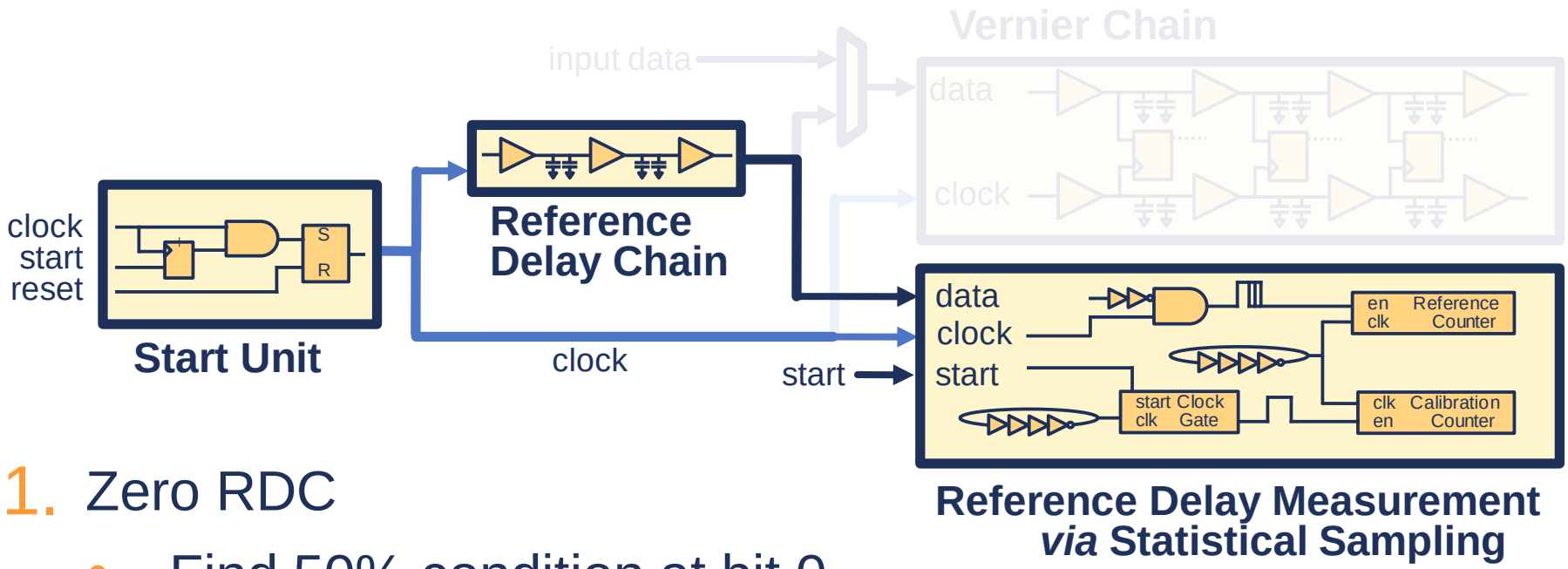
Statistical sampling provides **relative** delay measurements between RDC delays

# TDC Calibration




1. Zero RDC
   - Find 50% condition at bit 0

# TDC Calibration




1. Zero RDC
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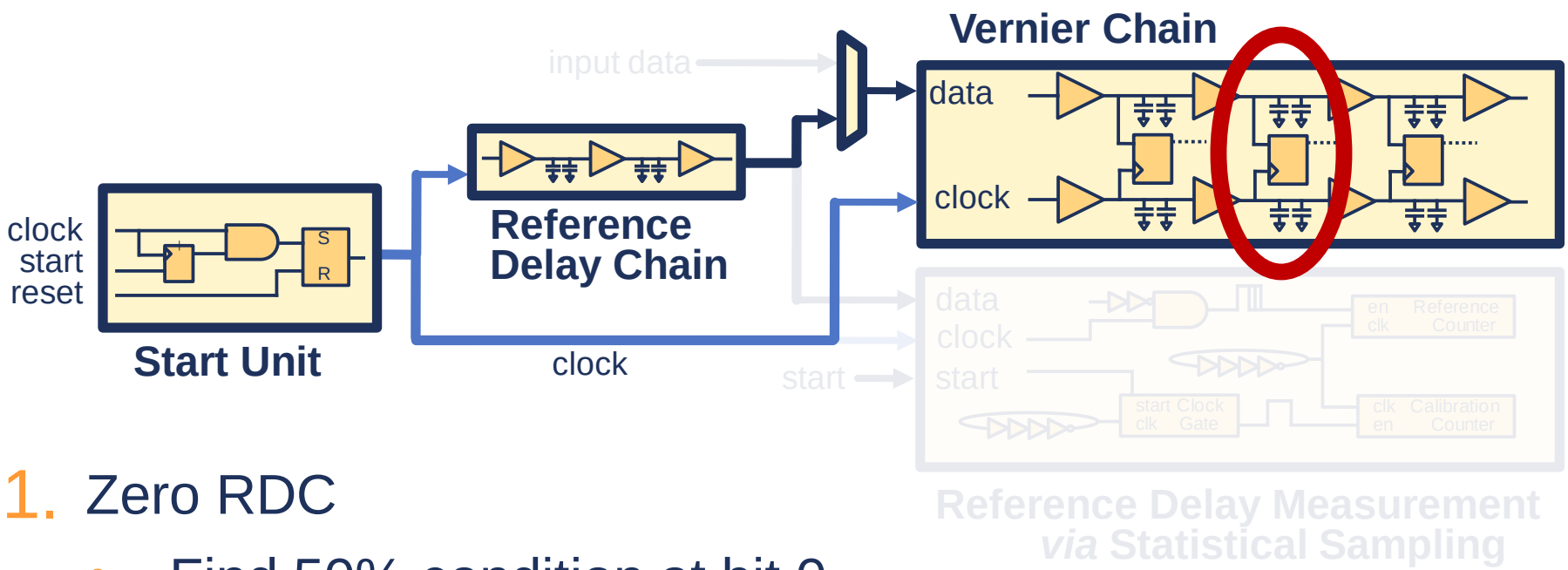
2. Increase RDC by 5ps

# TDC Calibration




1. Zero RDC
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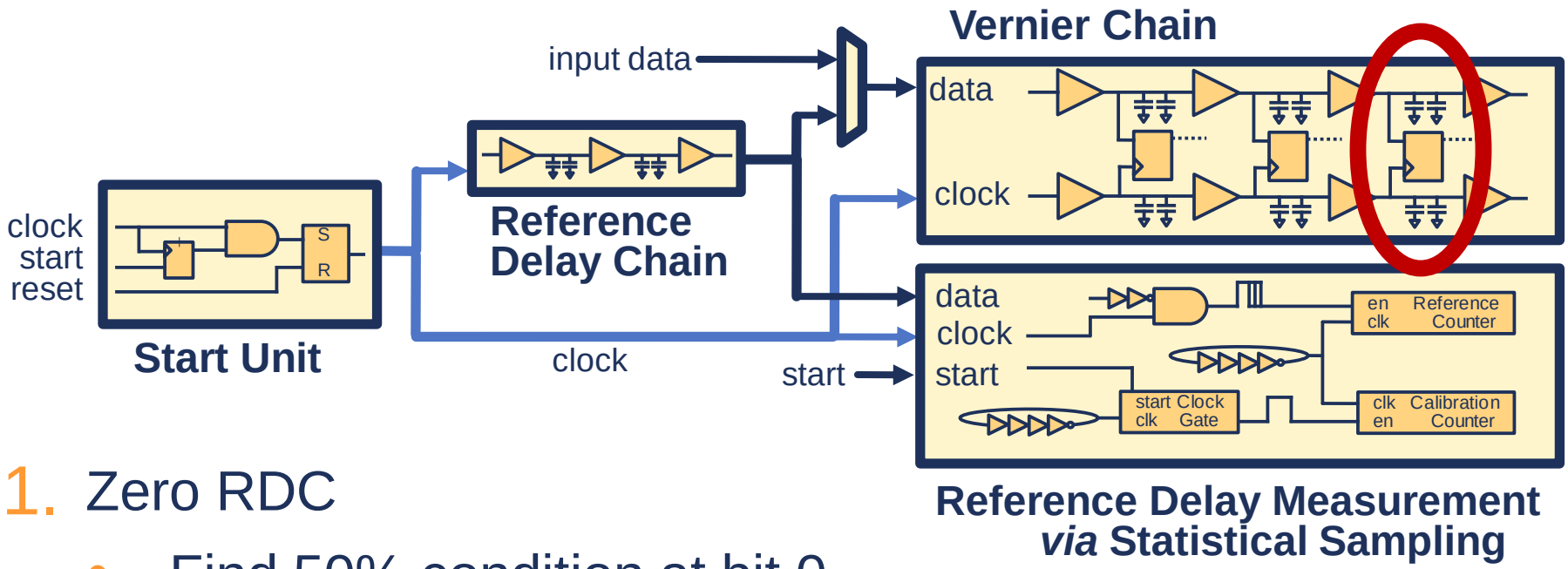
2. Increase RDC by 5ps (relative change)
3. Calibrate 1ps caps to meet 50% condition at the next bit

# TDC Calibration




1. Zero RDC
   - Find 50% condition at bit 0
2. Increase RDC by 5ps (relative change)
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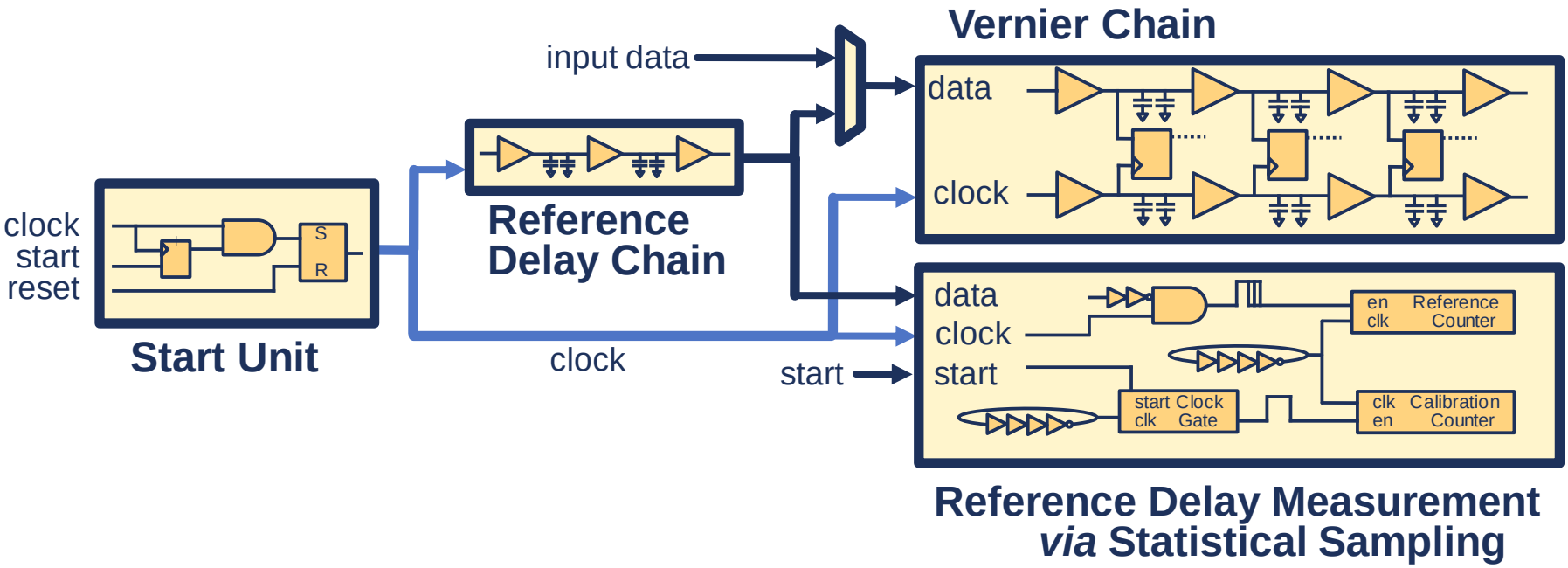
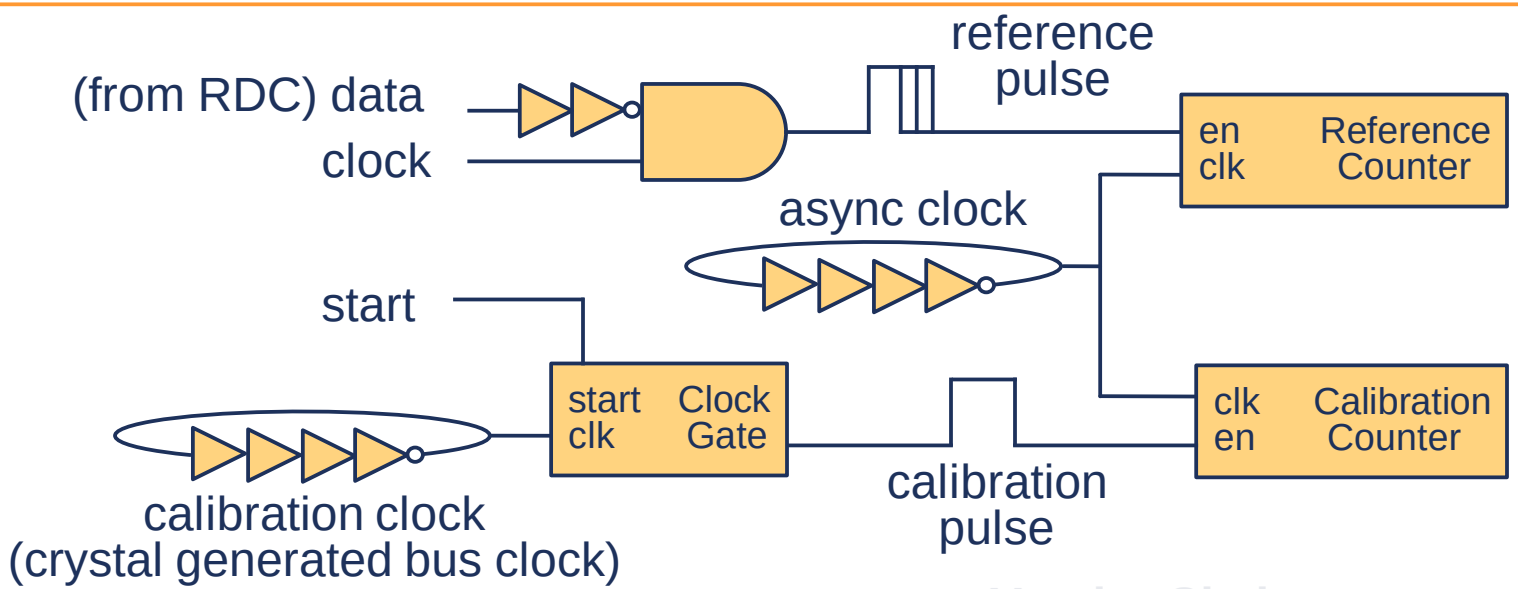
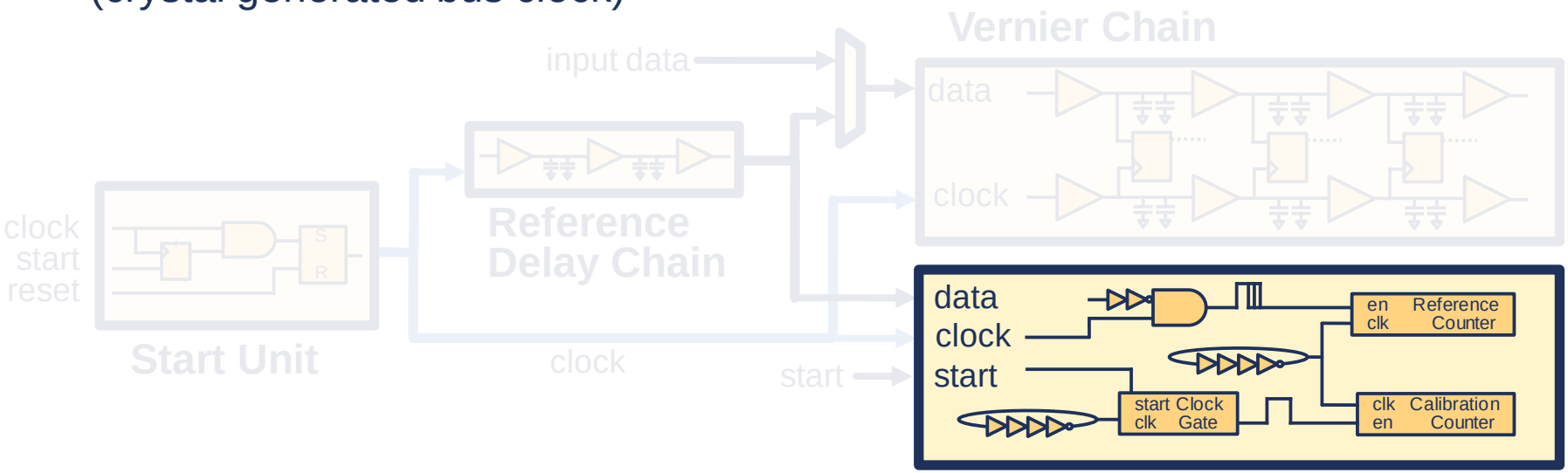
4. Repeat 2-3 for remaining bits

# TDC Components



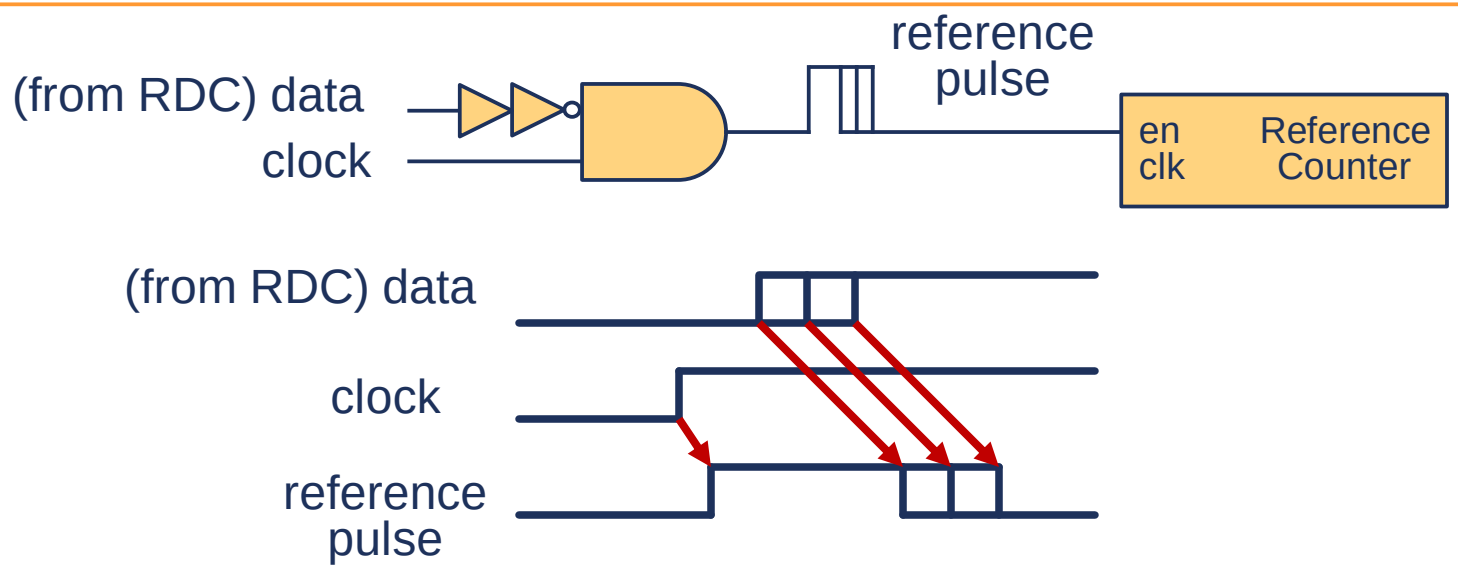
# TDC Delay Measurement

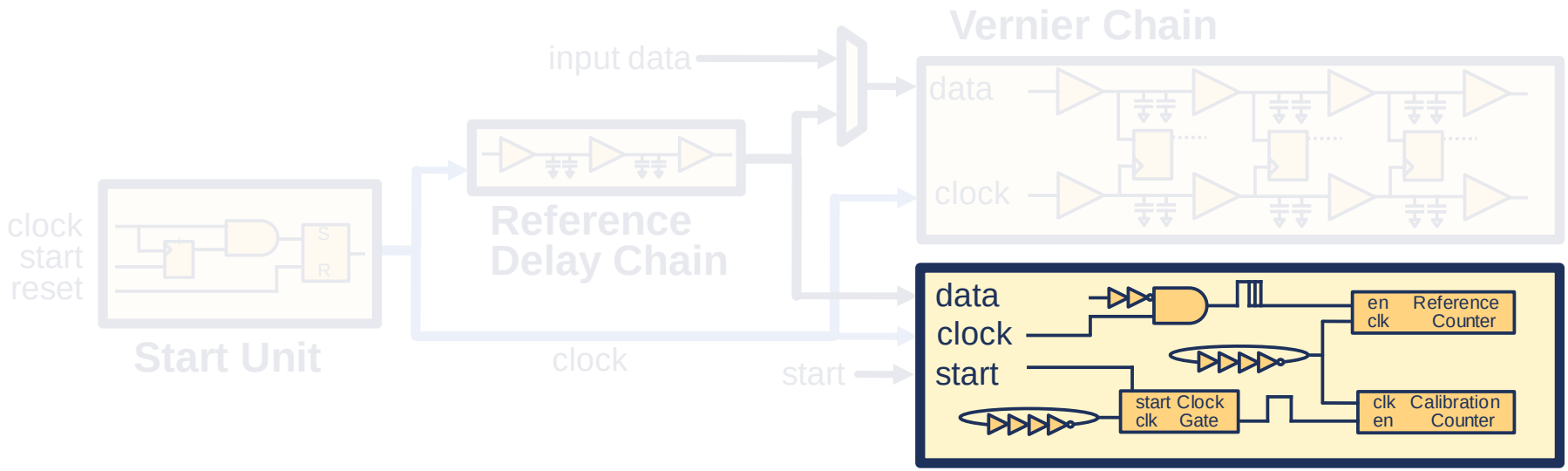



**Reference Delay Measurement *via* Statistical Sampling**

# TDC Delay Measurement

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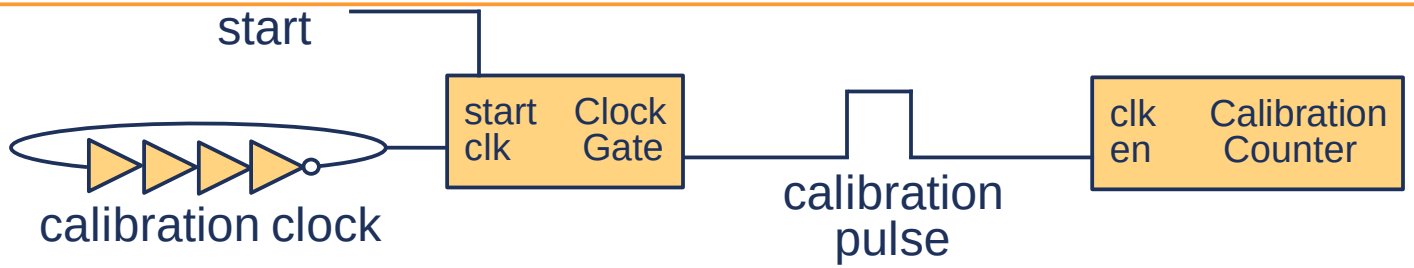


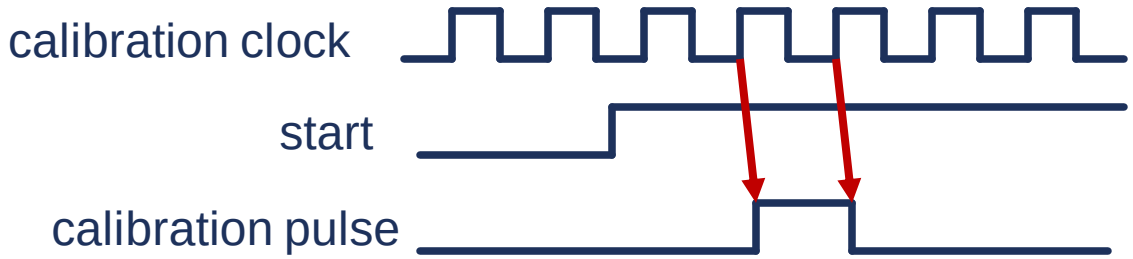


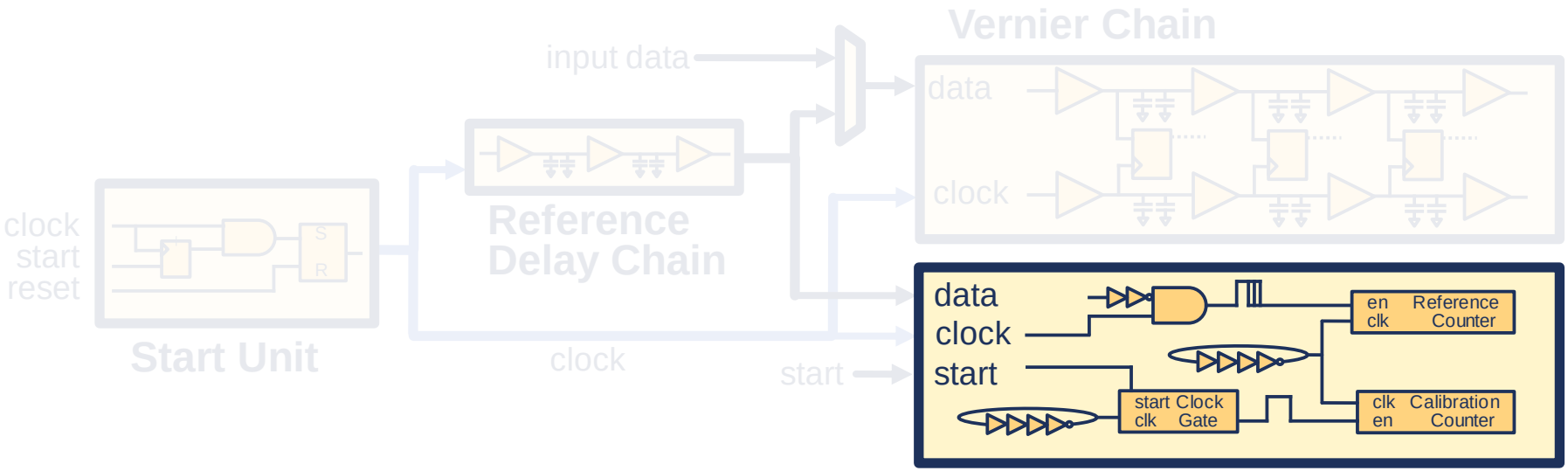


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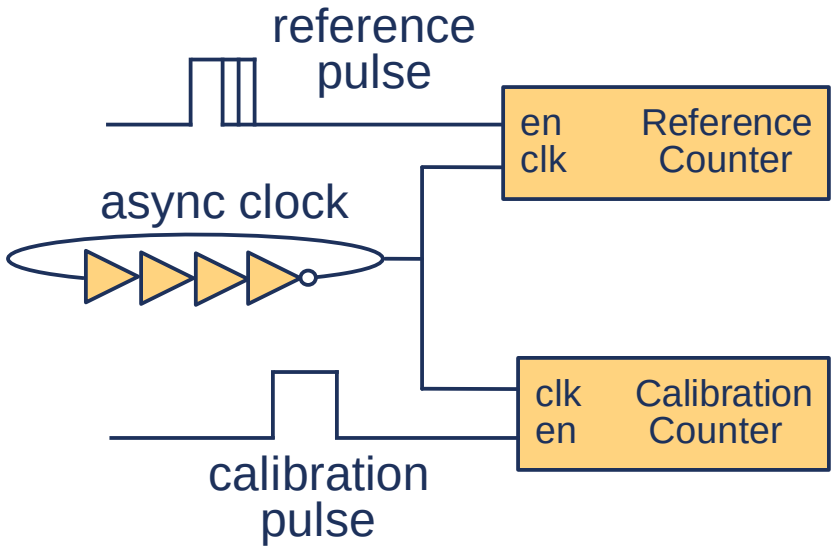
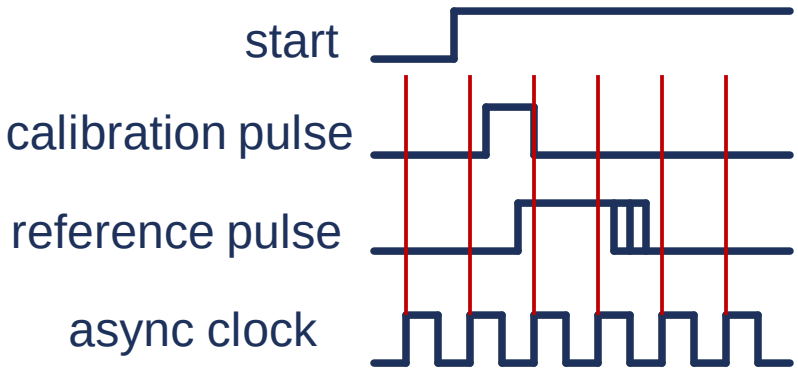
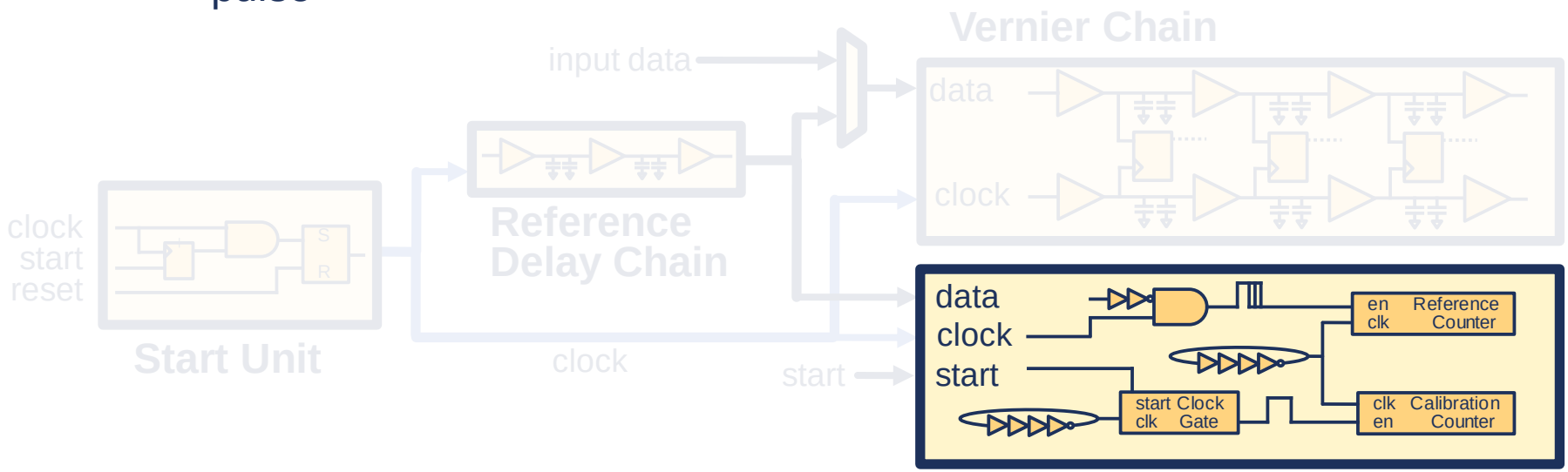
# TDC Delay Measurement

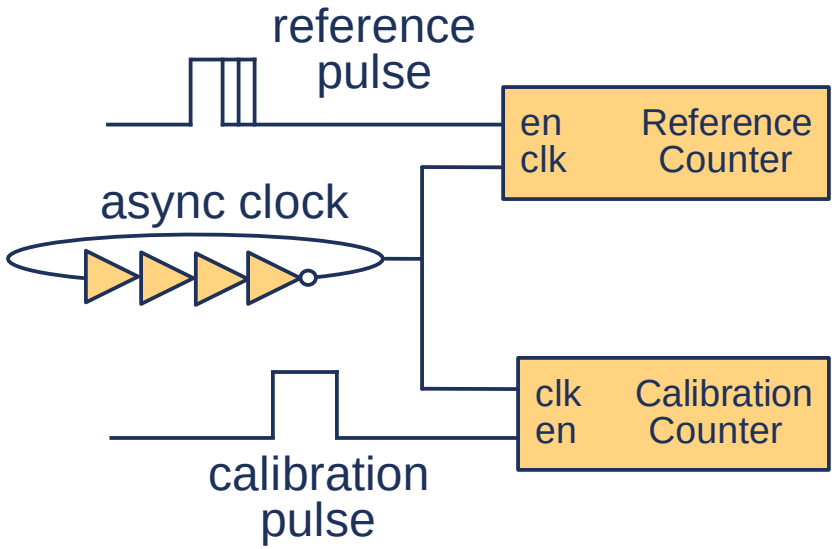


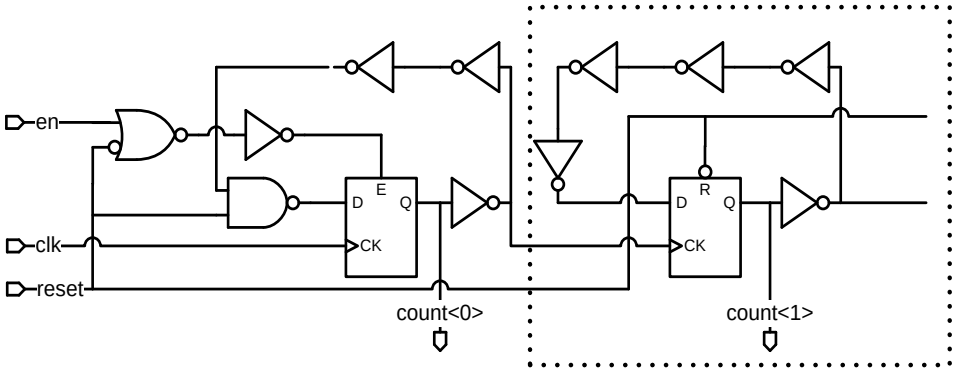



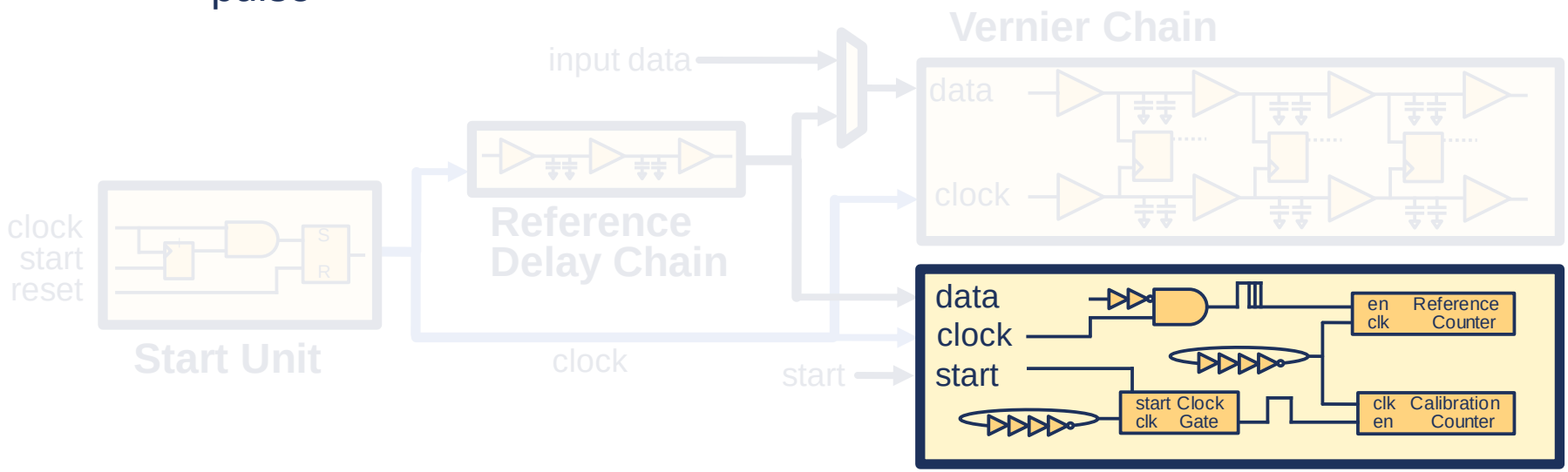




**Reference Delay Measurement *via* Statistical Sampling**

# TDC Delay Measurement

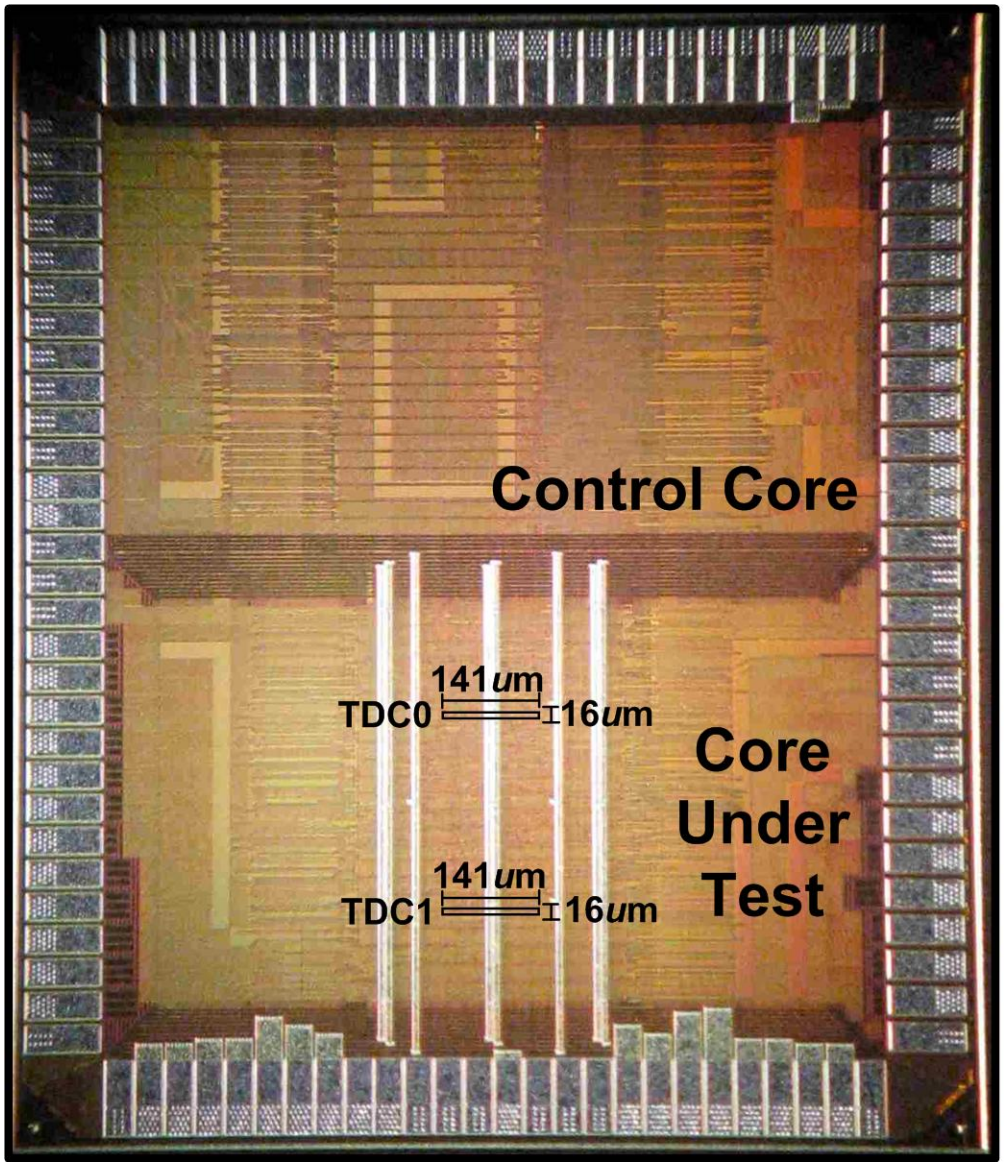


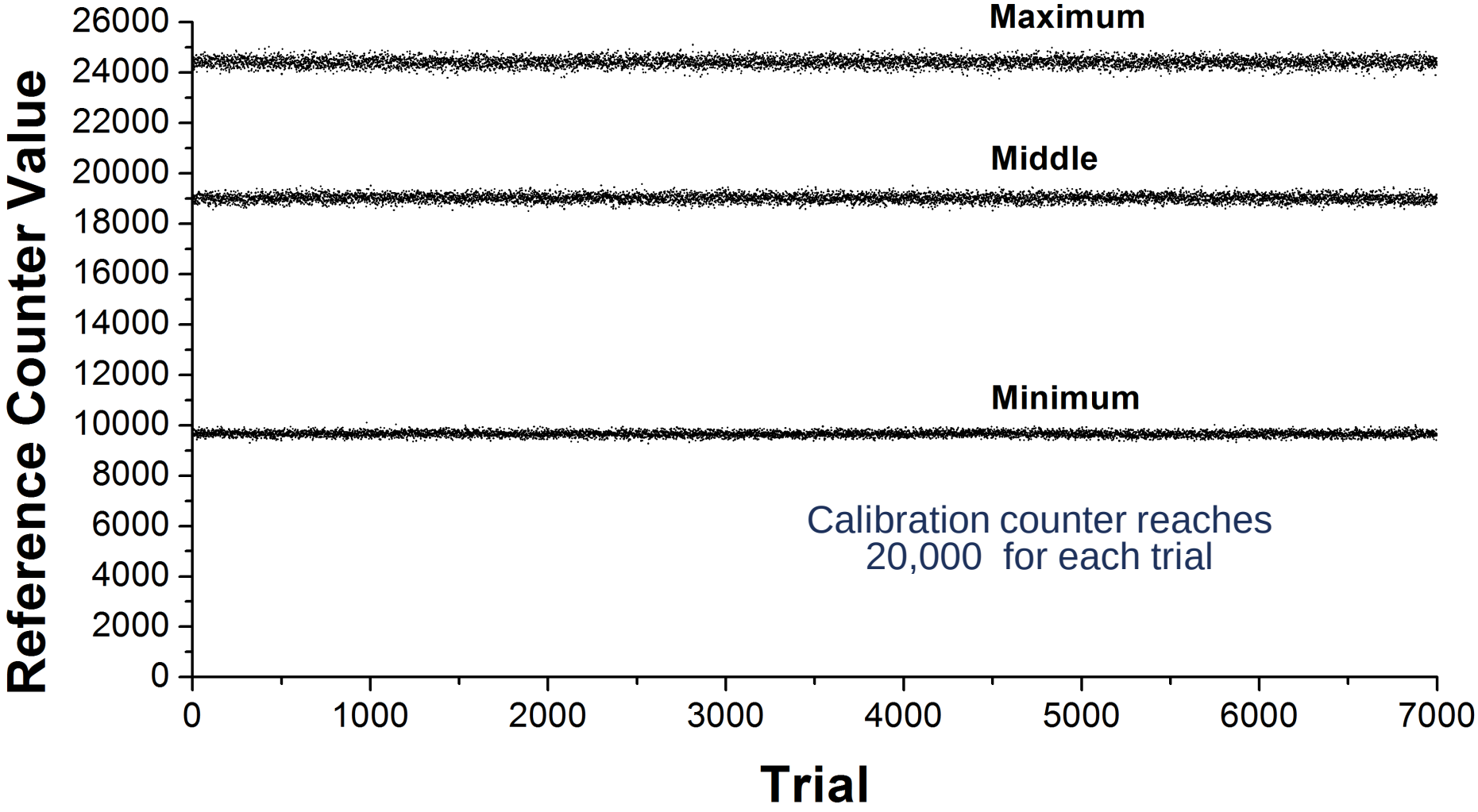

**Reference Delay Measurement *via* Statistical Sampling**

# Full Chip Floorplan

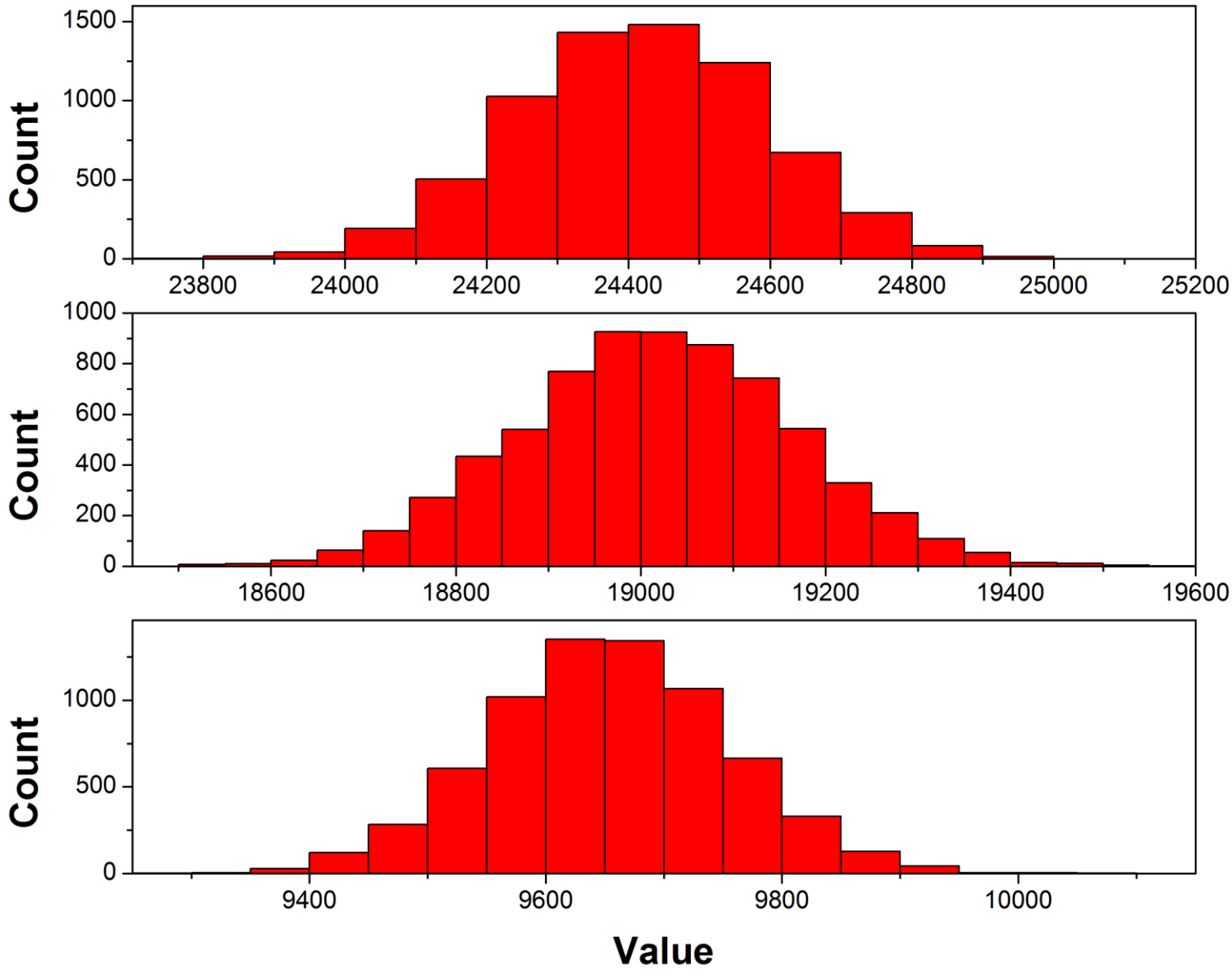



| | |
|---|---|
| Technology | ST45 LP,<br>1.1 volt |
| TDC Area | 141umx16um<br>0.00225 $mm^2$ |
| Chip Area | 1.5mmx1.3mm |
| Test Core | 64-bit alpha<br>7-stage<br>in-order<br>400 MHz |

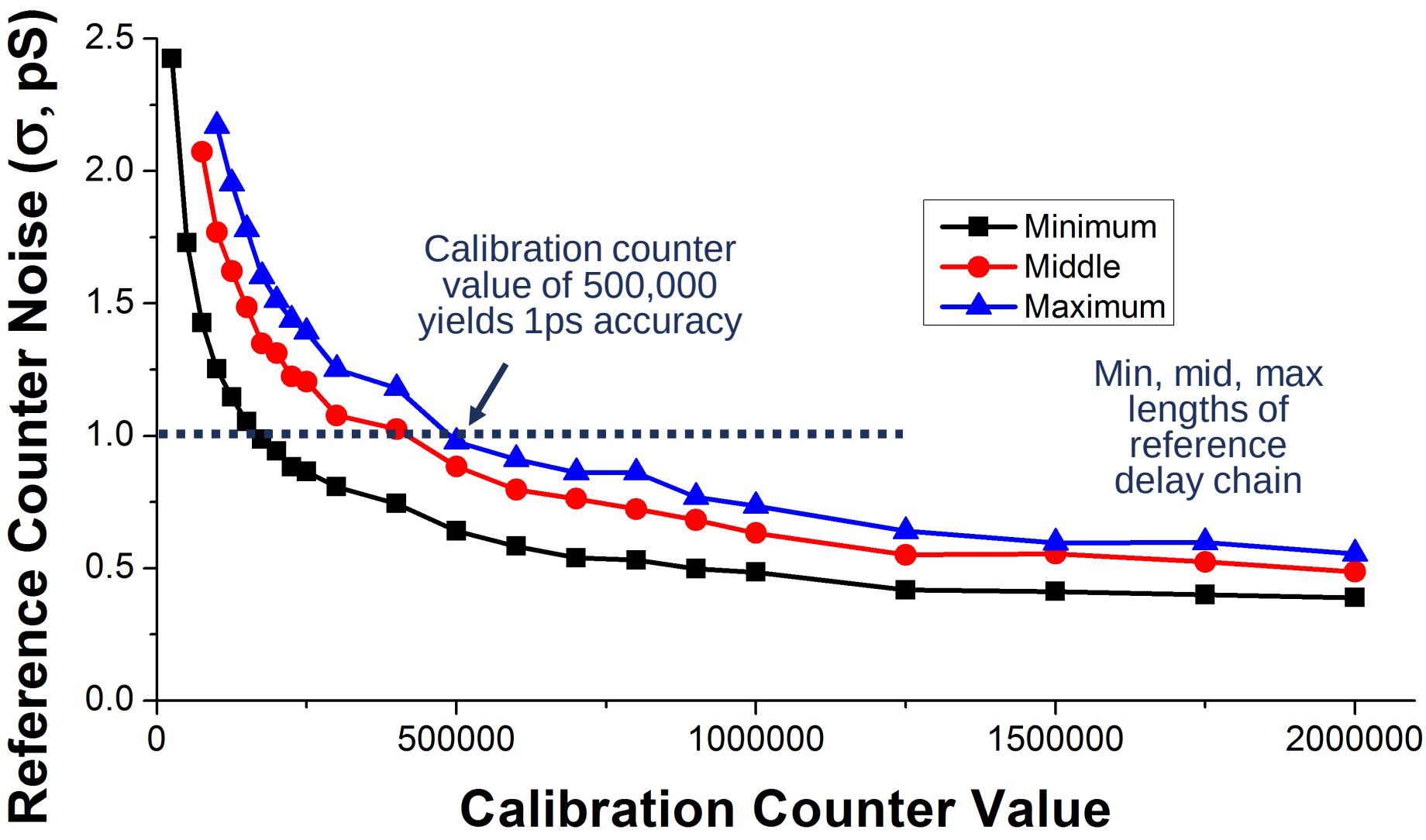
# TDC Statistical Sampling Results



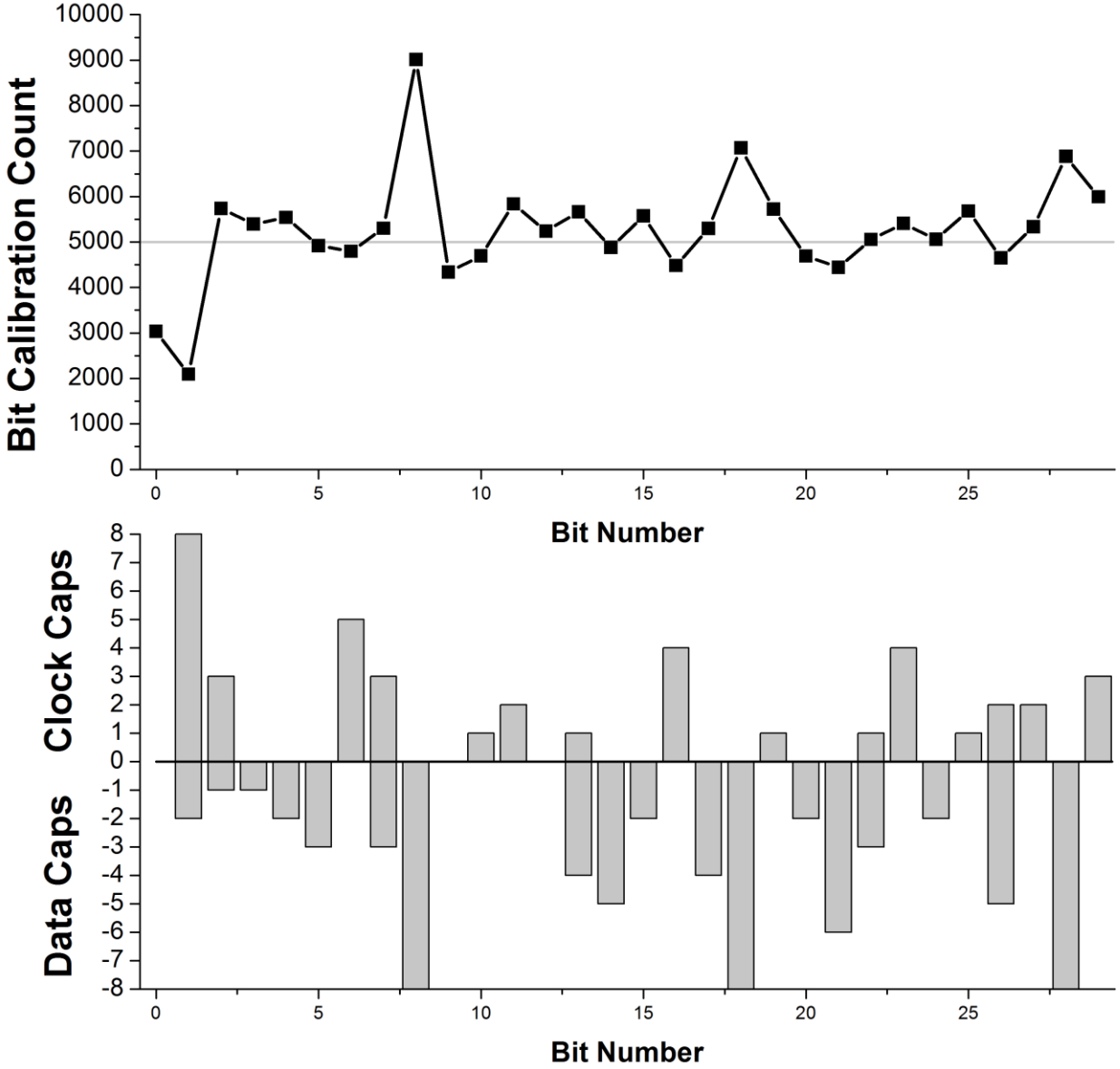
# TDC Statistical Sampling Results



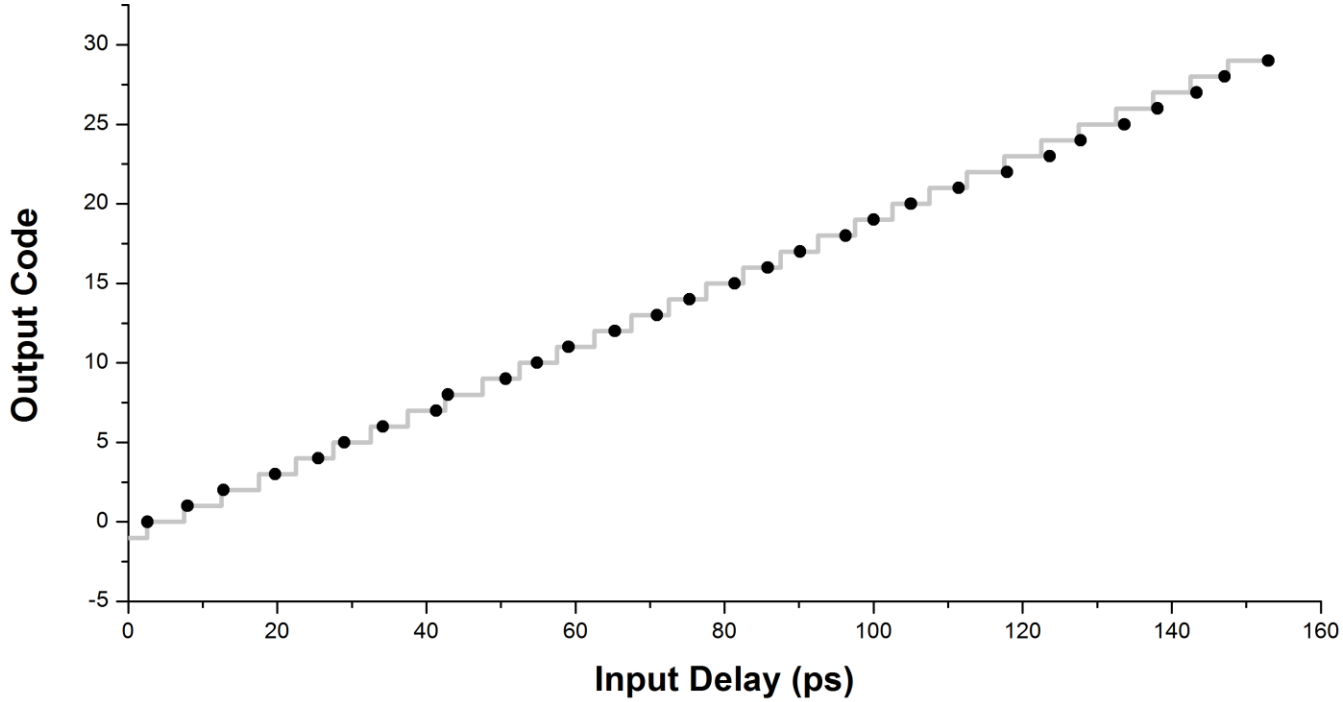
# TDC Statistical Sampling Results



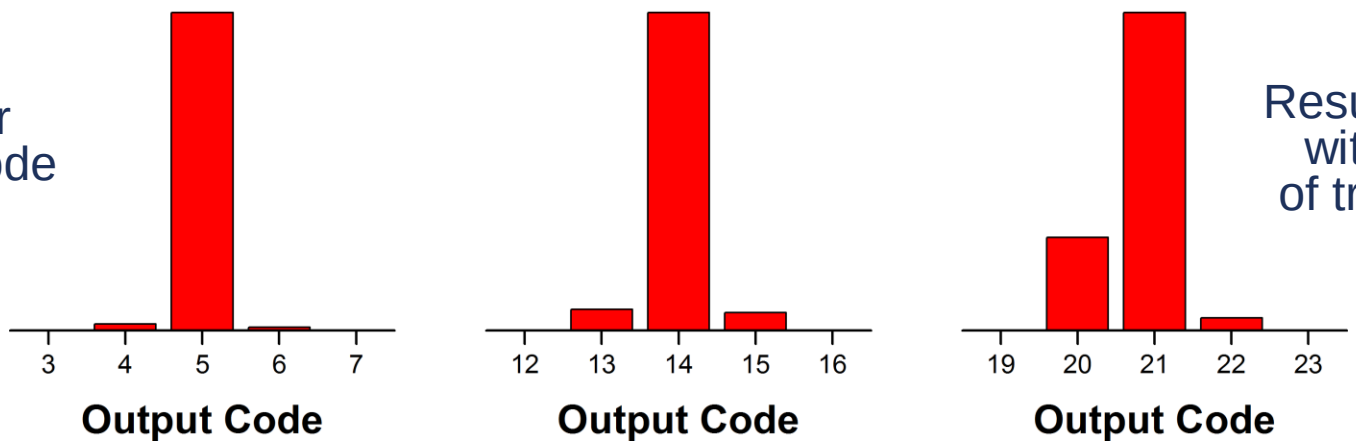
# TDC Calibration Results



# TDC Calibration Results

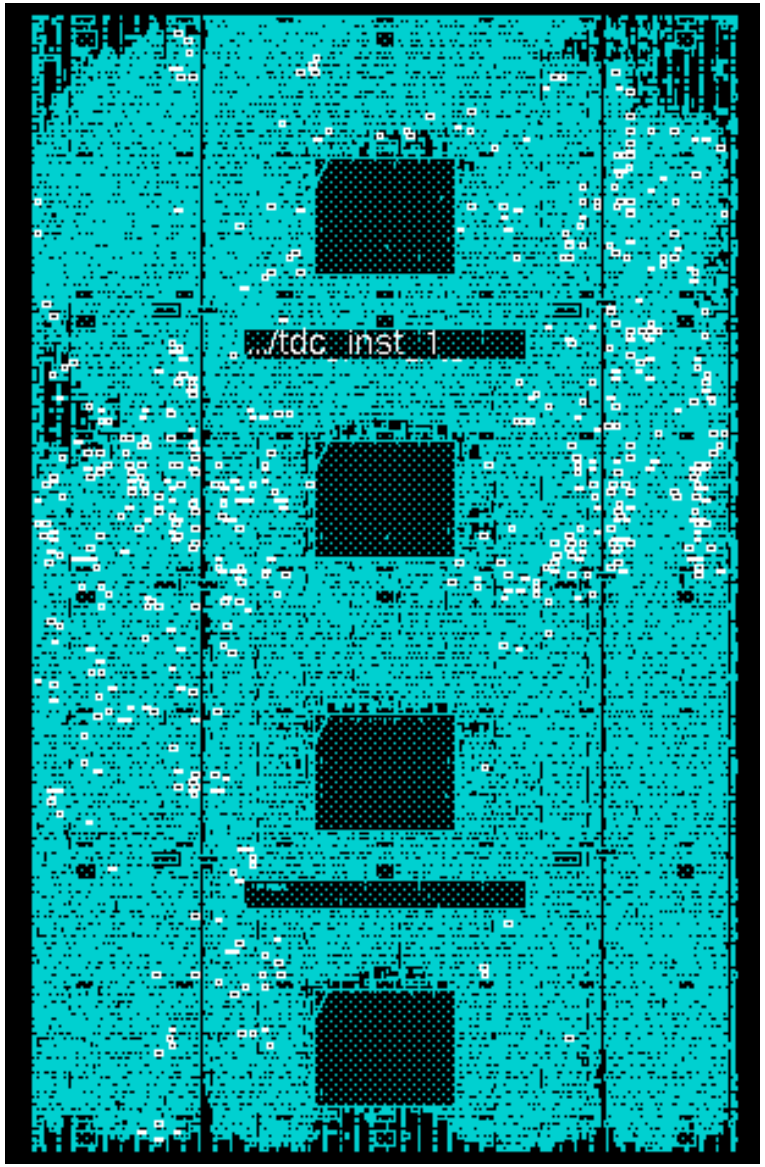



5ps per output code



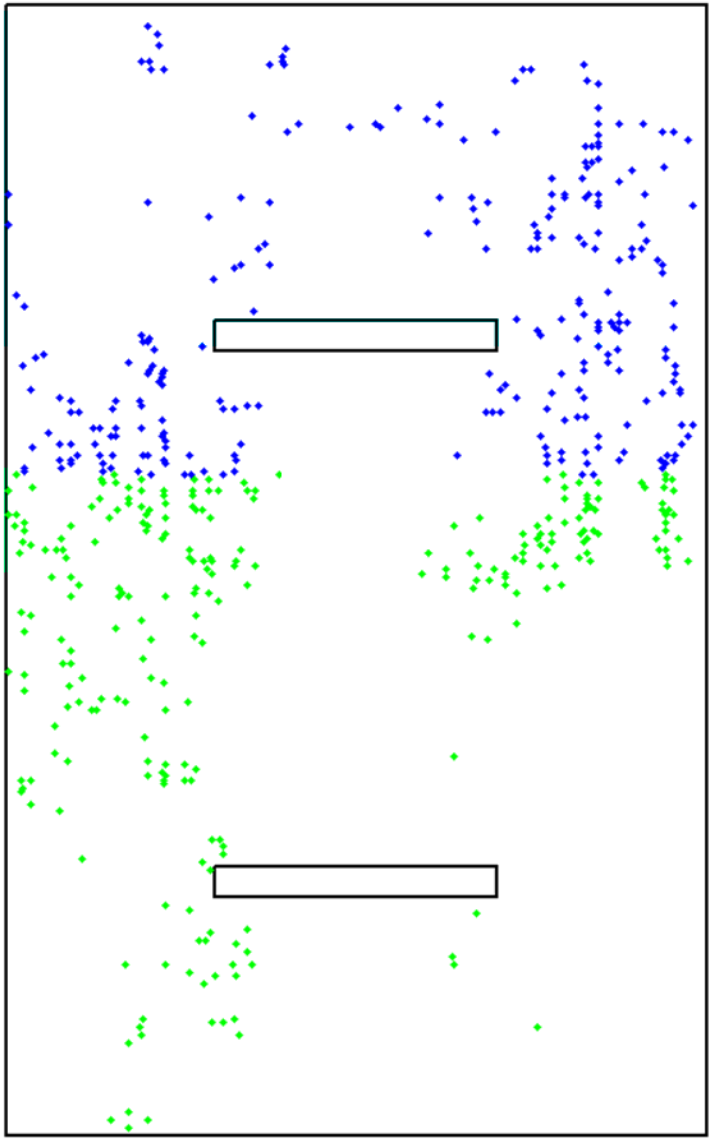

Result always within 5ps of true value

# Monitored Register Locations



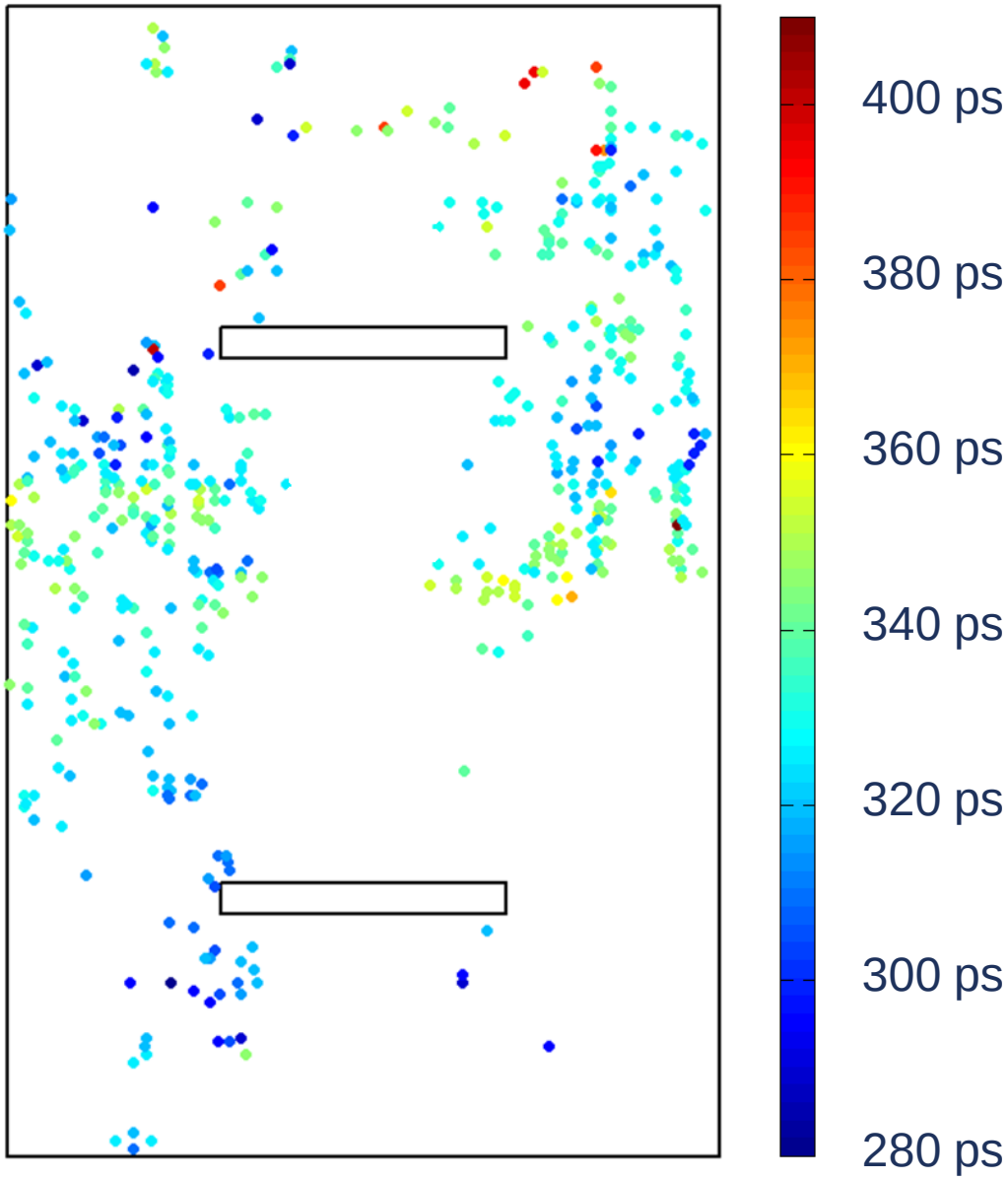

- Monitored top 512 flops
- Muxes inserted via ECO after routing using Cadence Encounter

# Monitored Register Locations

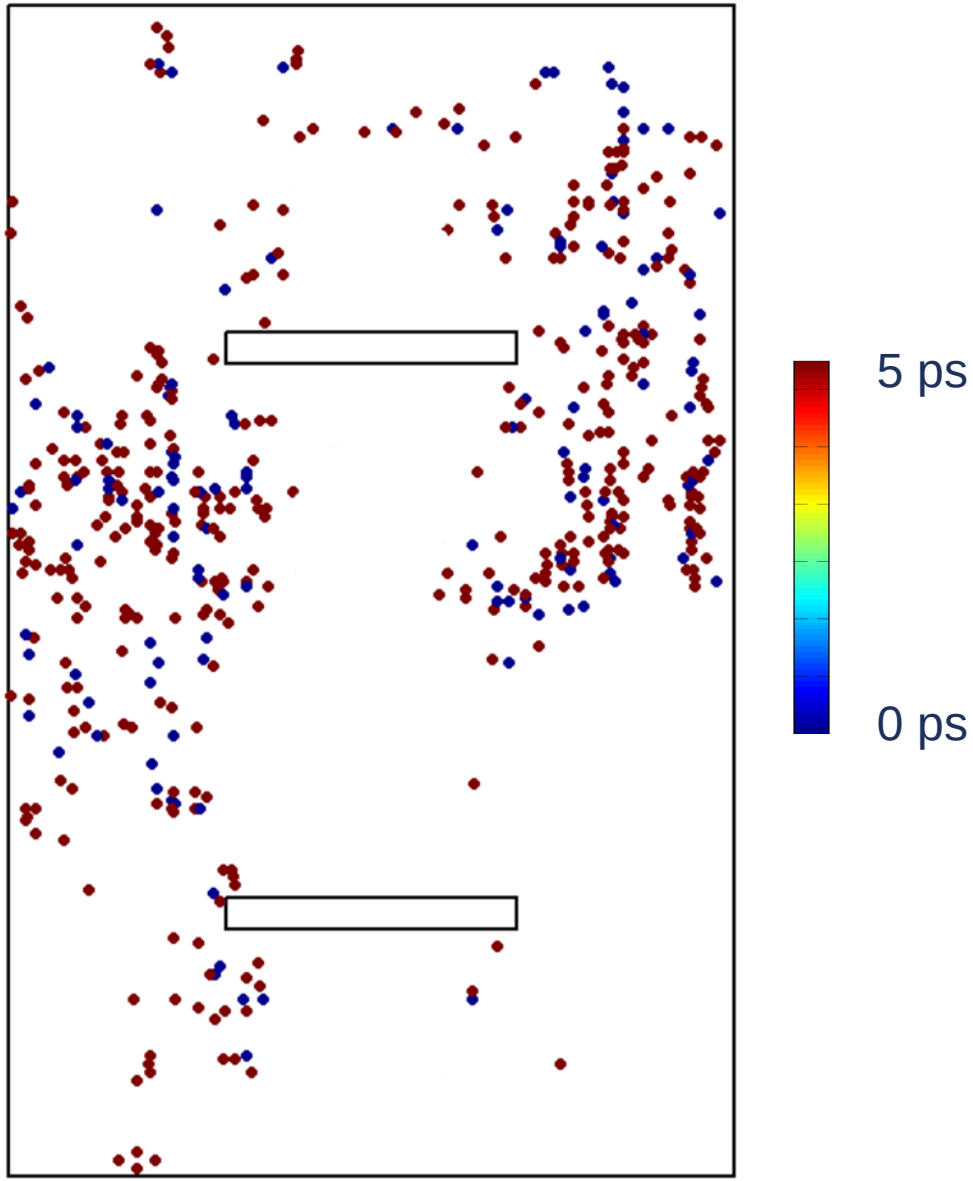


- Monitored top 512 flops
- Muxes inserted via ECO after routing using Cadence Encounter

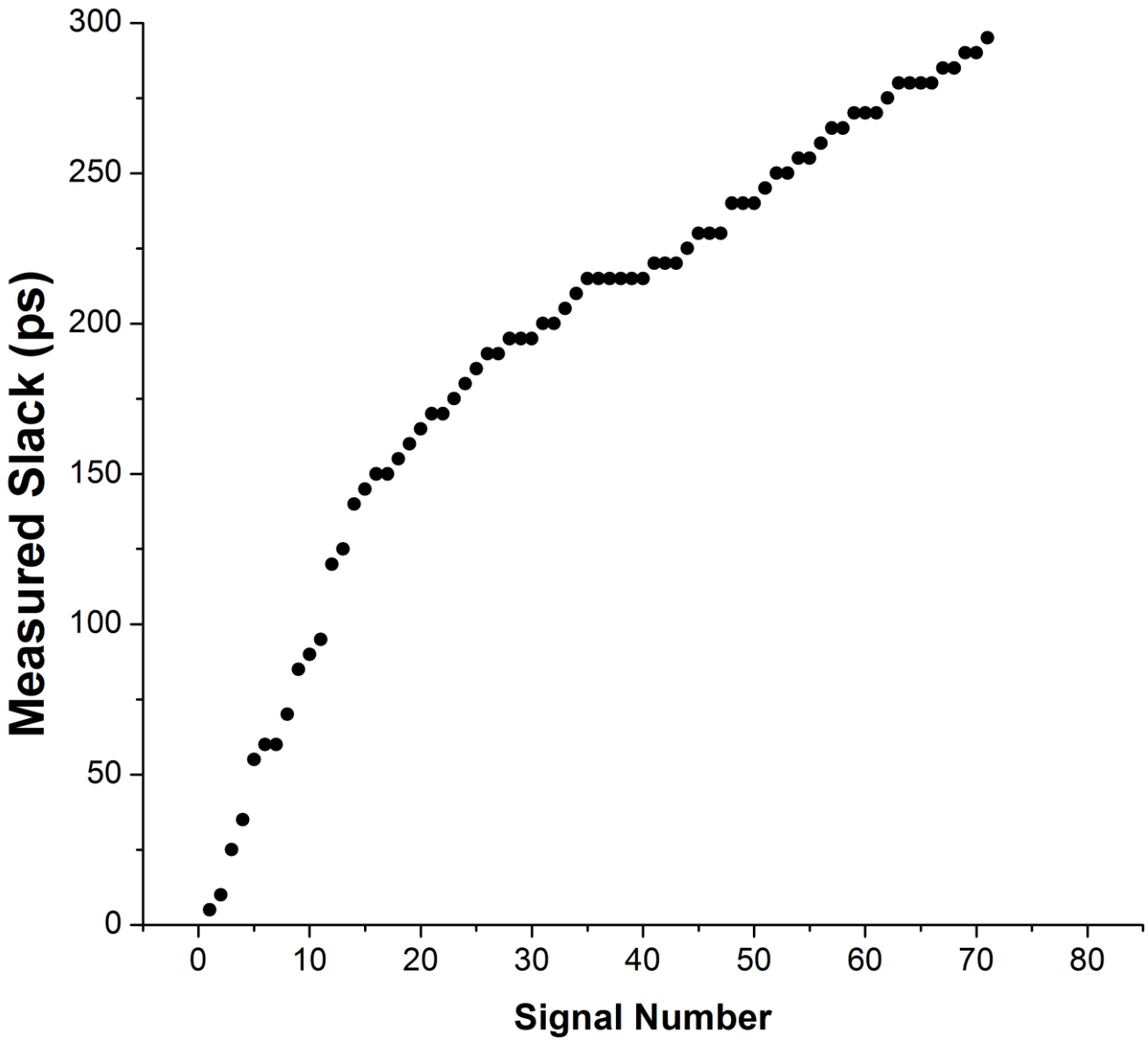
# Clock Latencies



# Clock Latencies – Multiple Trials



# Pipeline Measurement Results



# Summary

- A novel time-to-digital architecture
- Includes high-accuracy calibration via statistical sampling
- Suitable for high-performance delay-slack monitoring
- Future work: Safety Razor
- We thank:
  - STMicroelectronics for fabrication
  - ARM Ltd for support and suggestions