Millimeter-Scale Nearly Perpetual Sensor System with Stacked Battery and Solar Cells

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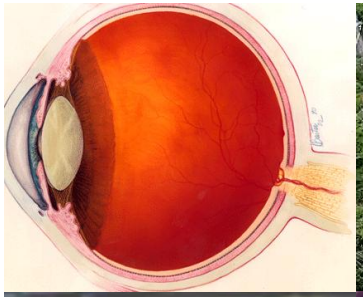
Electrical Engineering & Computer Science Department
The University of Michigan, Ann Arbor

Motivation

Long Device Lifetime
Small Form Factor

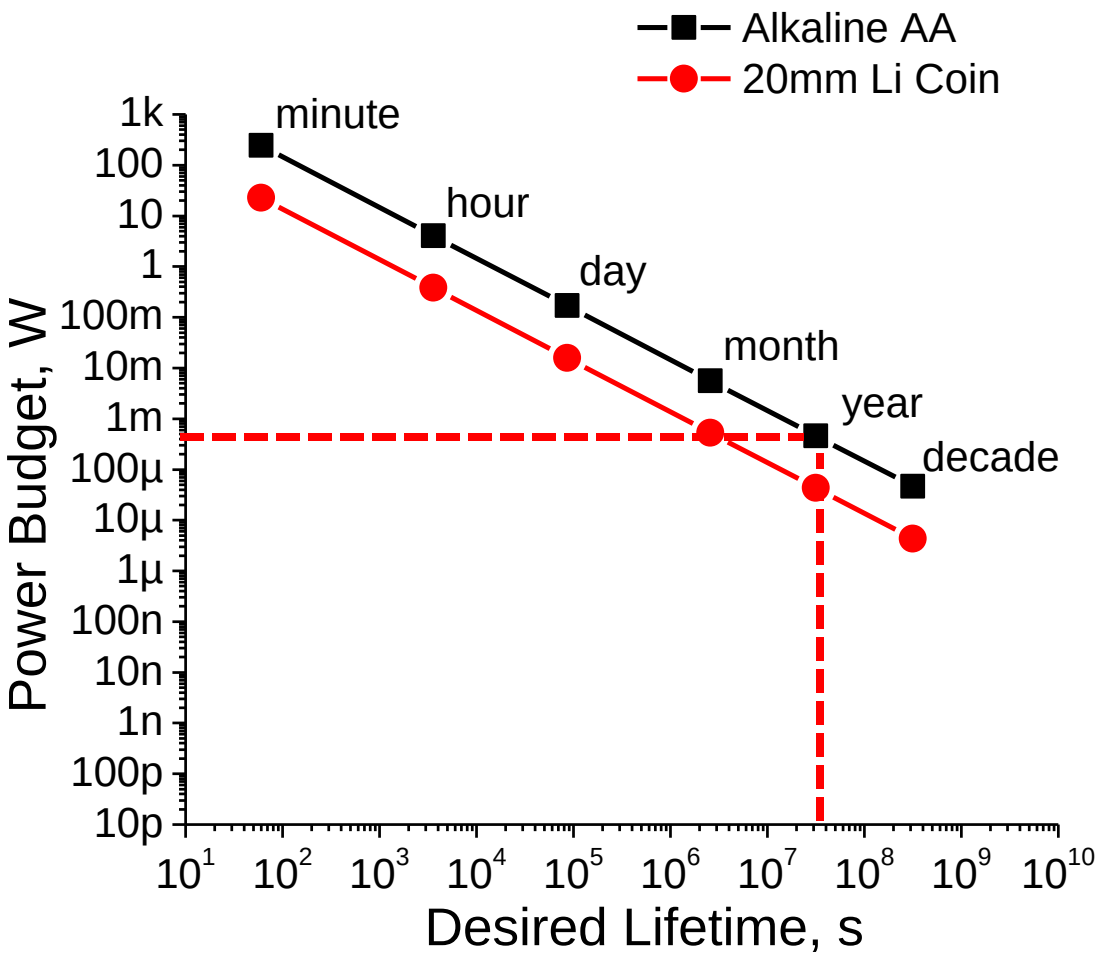
Implantable Medical Devices



Infrastructure Monitoring

Military Surveillance

Smart RFID



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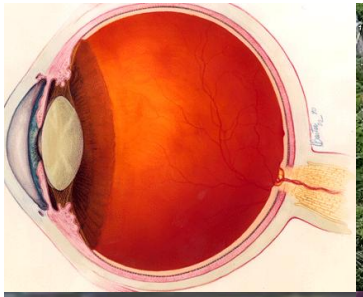

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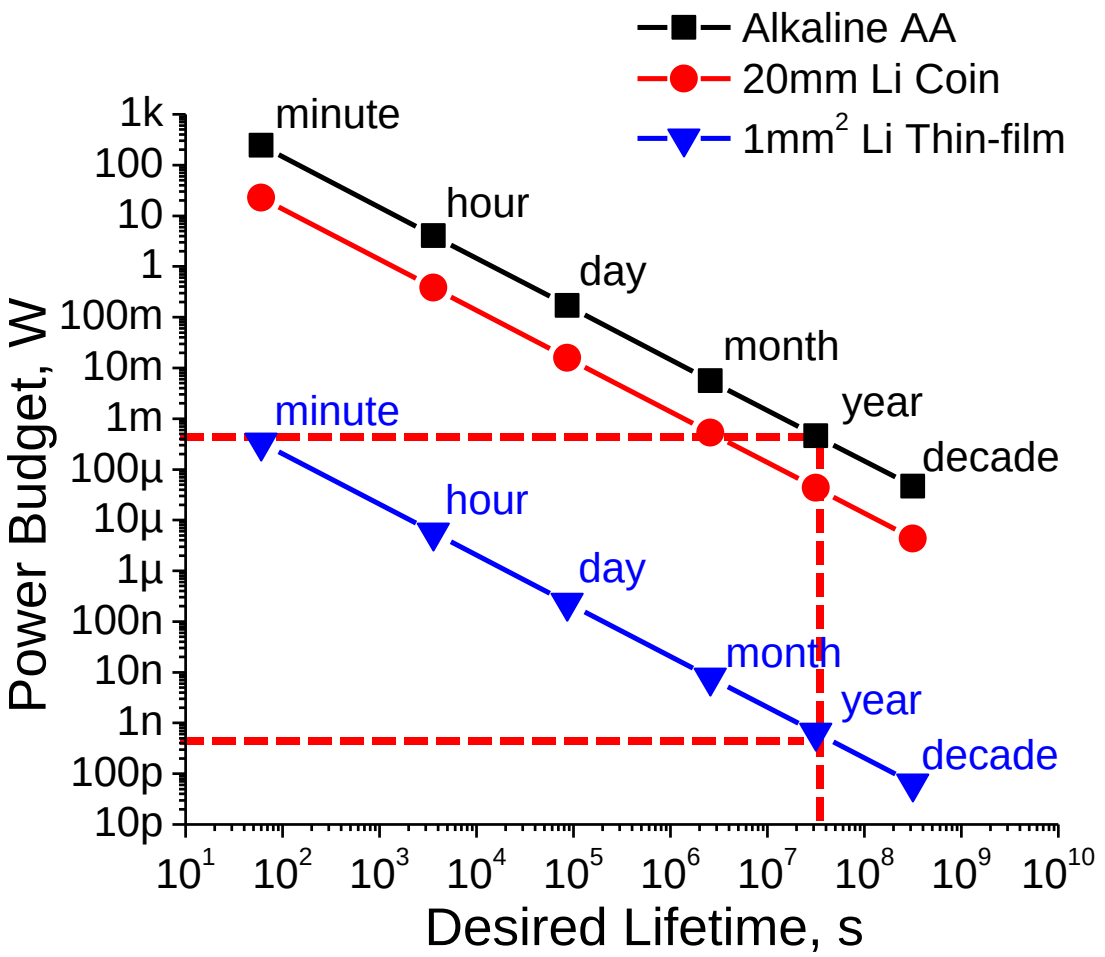
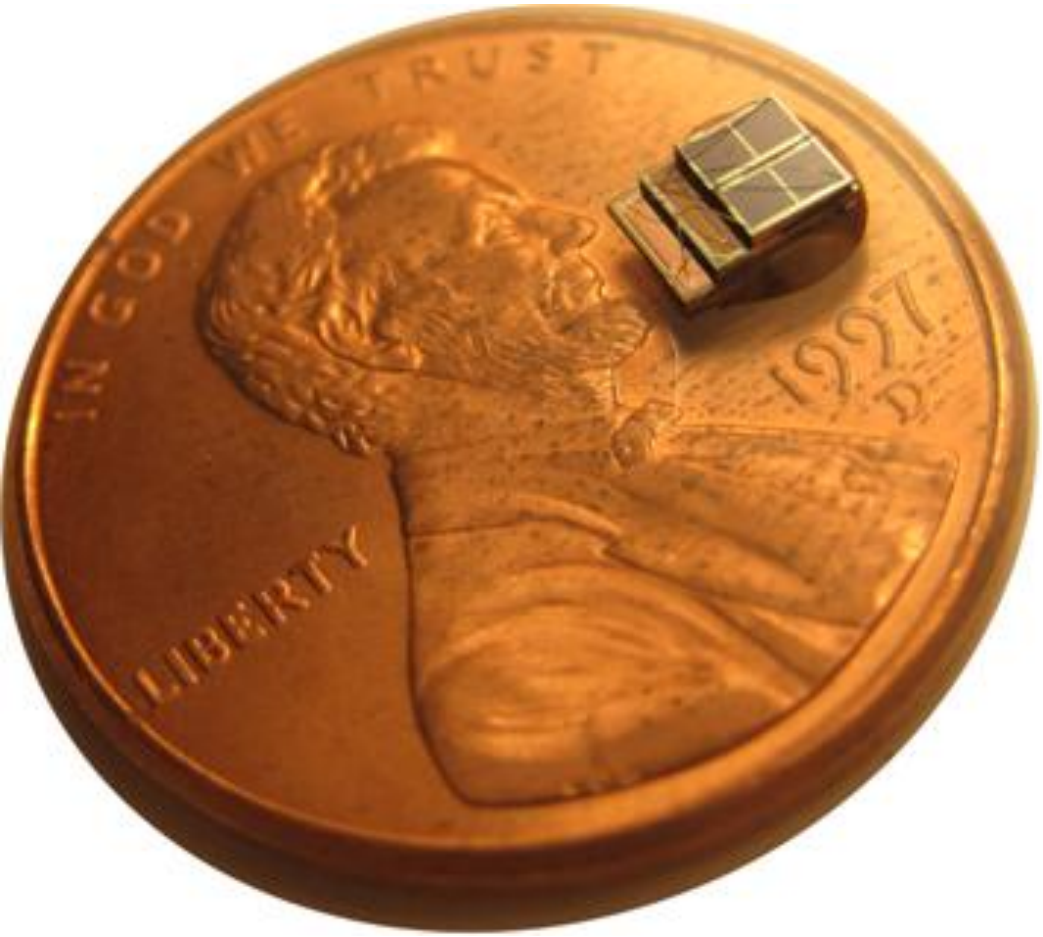
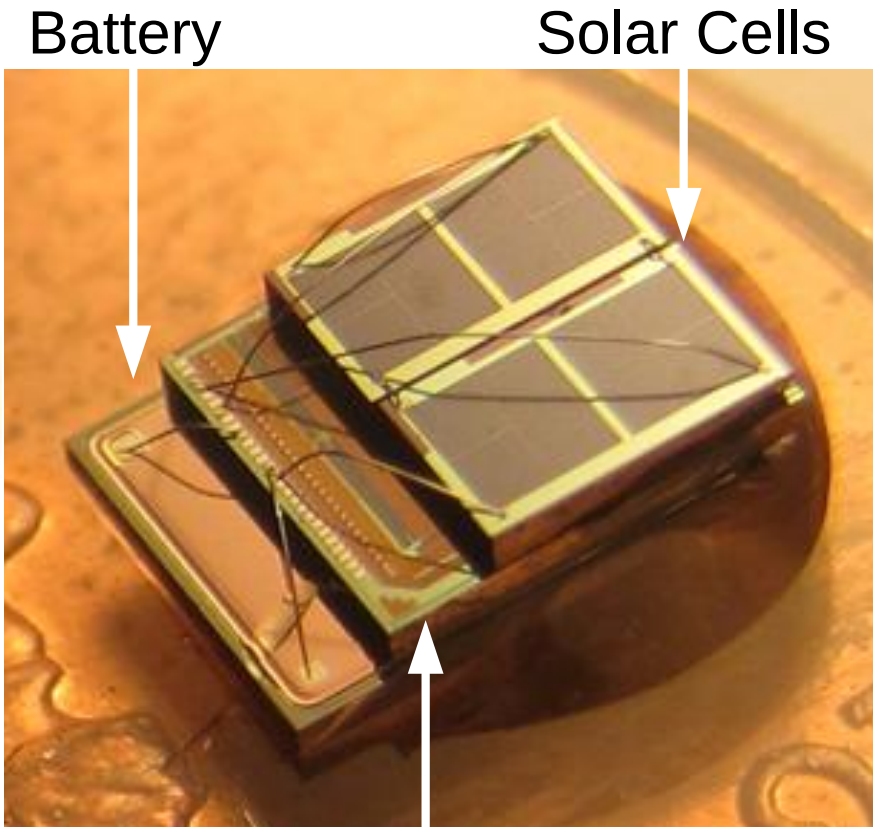


8.75mm^3 Sensor System

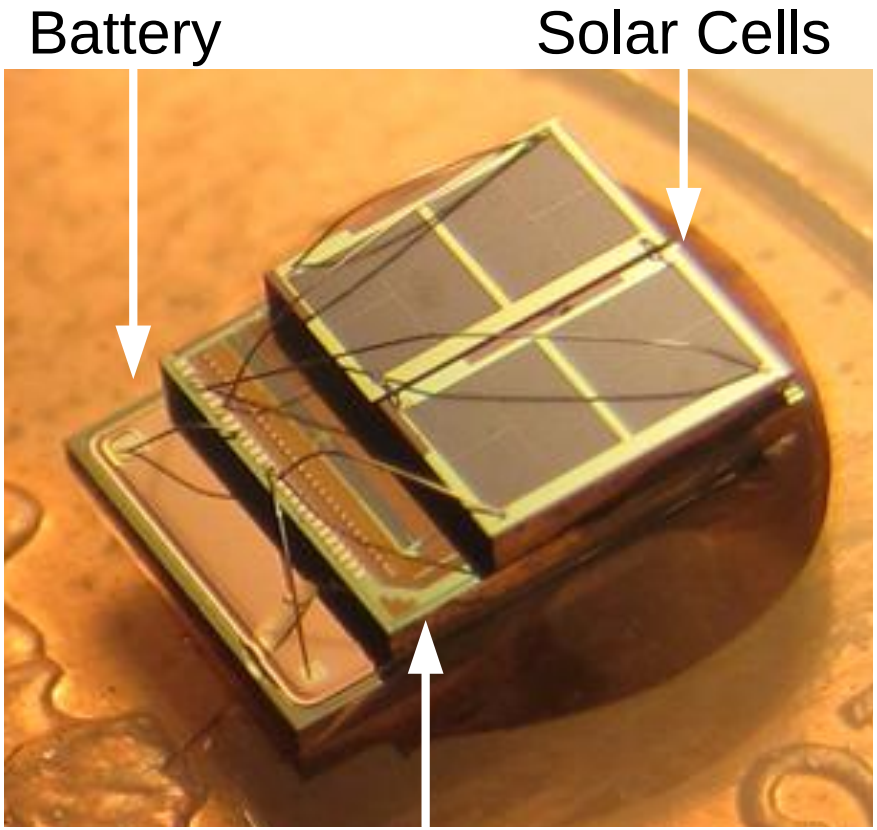




Processor, SRAM and PMU

8.75mm³ Sensor System

- Solar cells
  - 2 series solar cells
  - 0.18 µm CMOS
  - Removed nitride and silicide
- Battery
  - 3.6 V Cymbet thin-film Li
  - 12 µAh capacity
  - 2.5 mm x 3.5 mm
- Integrated circuits
  - Near-threshold Cortex-M3
  - Low-voltage SRAM
  - Power Management Unit



Processor, SRAM and PMU

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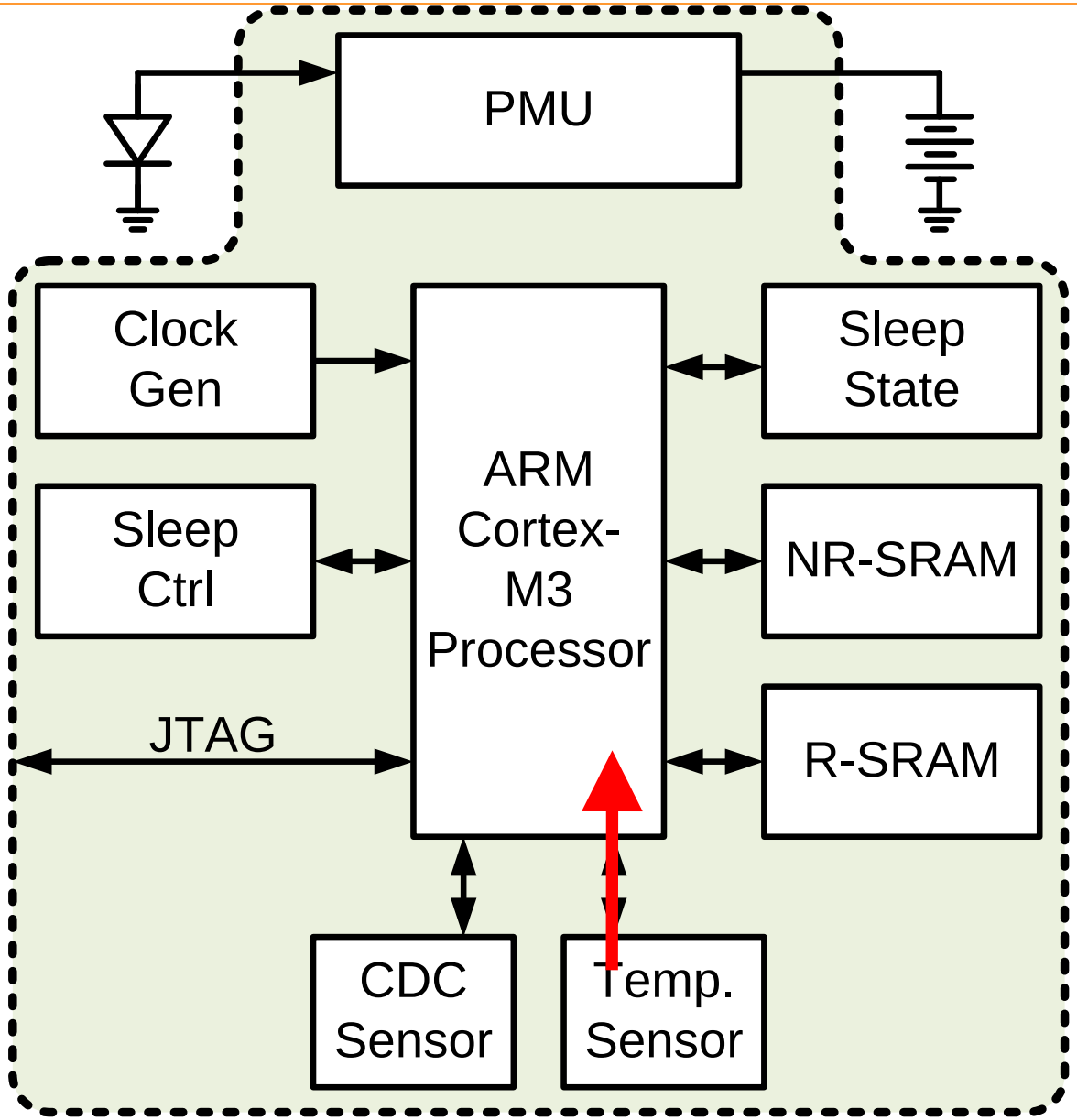

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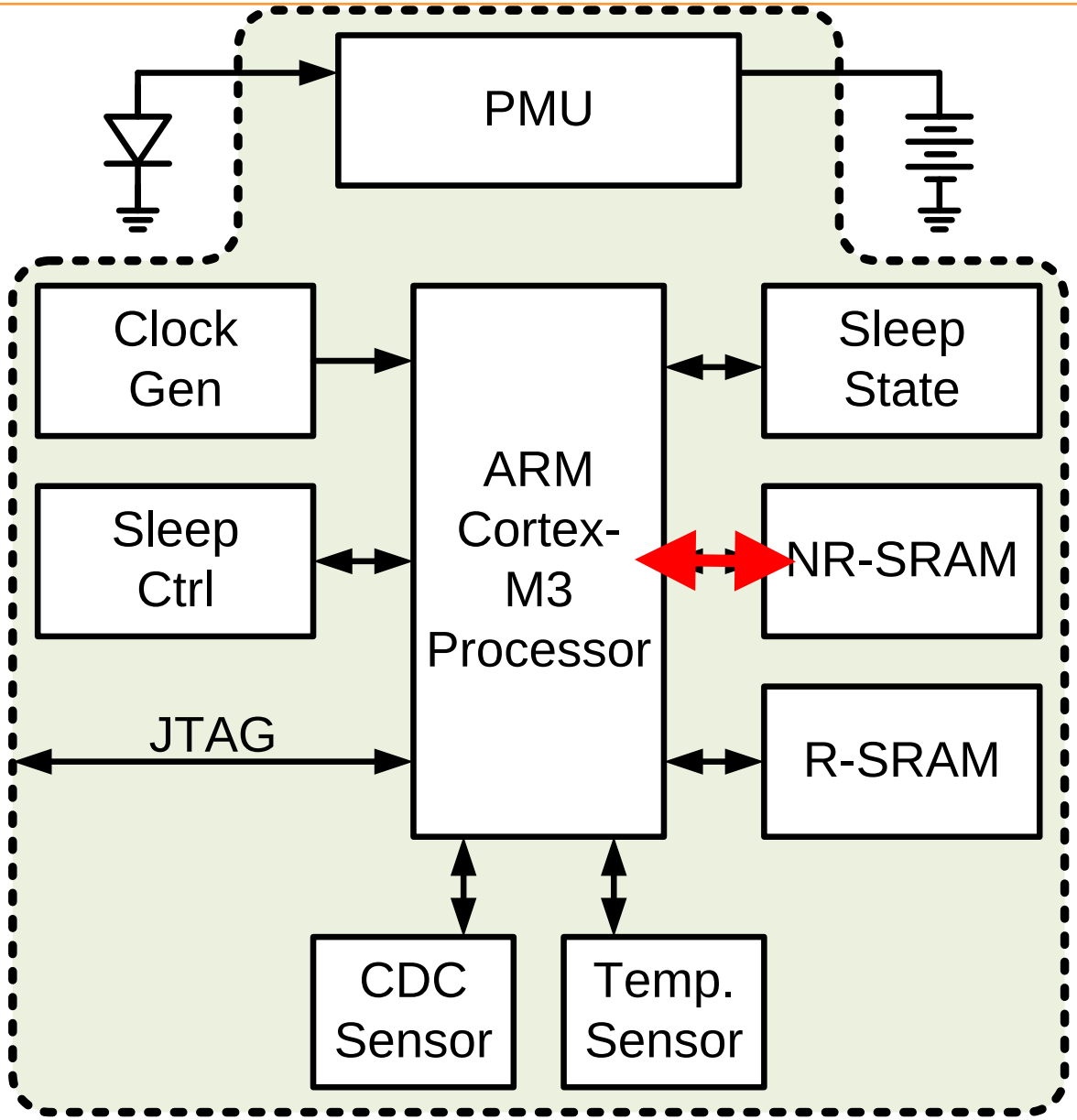

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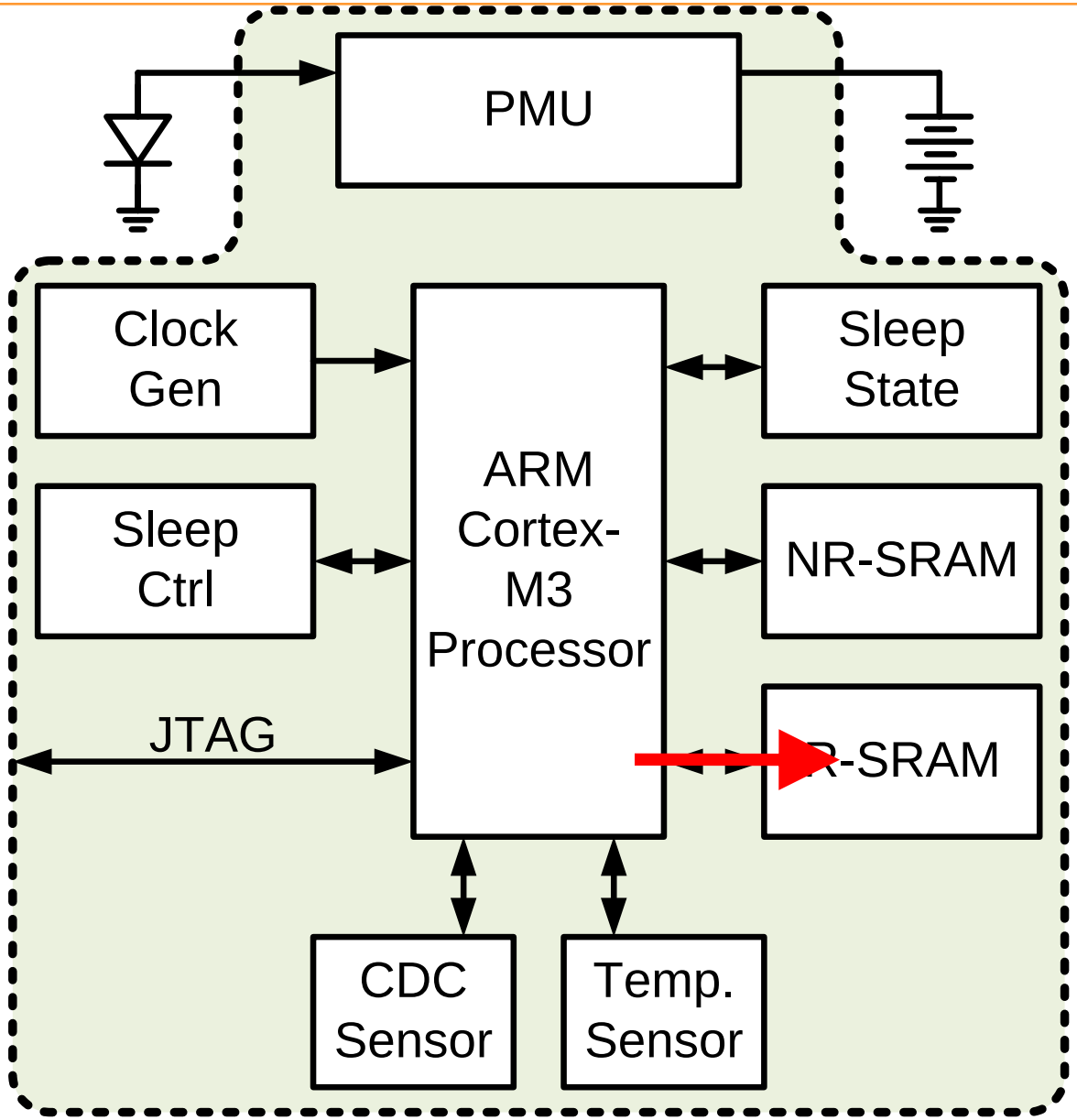

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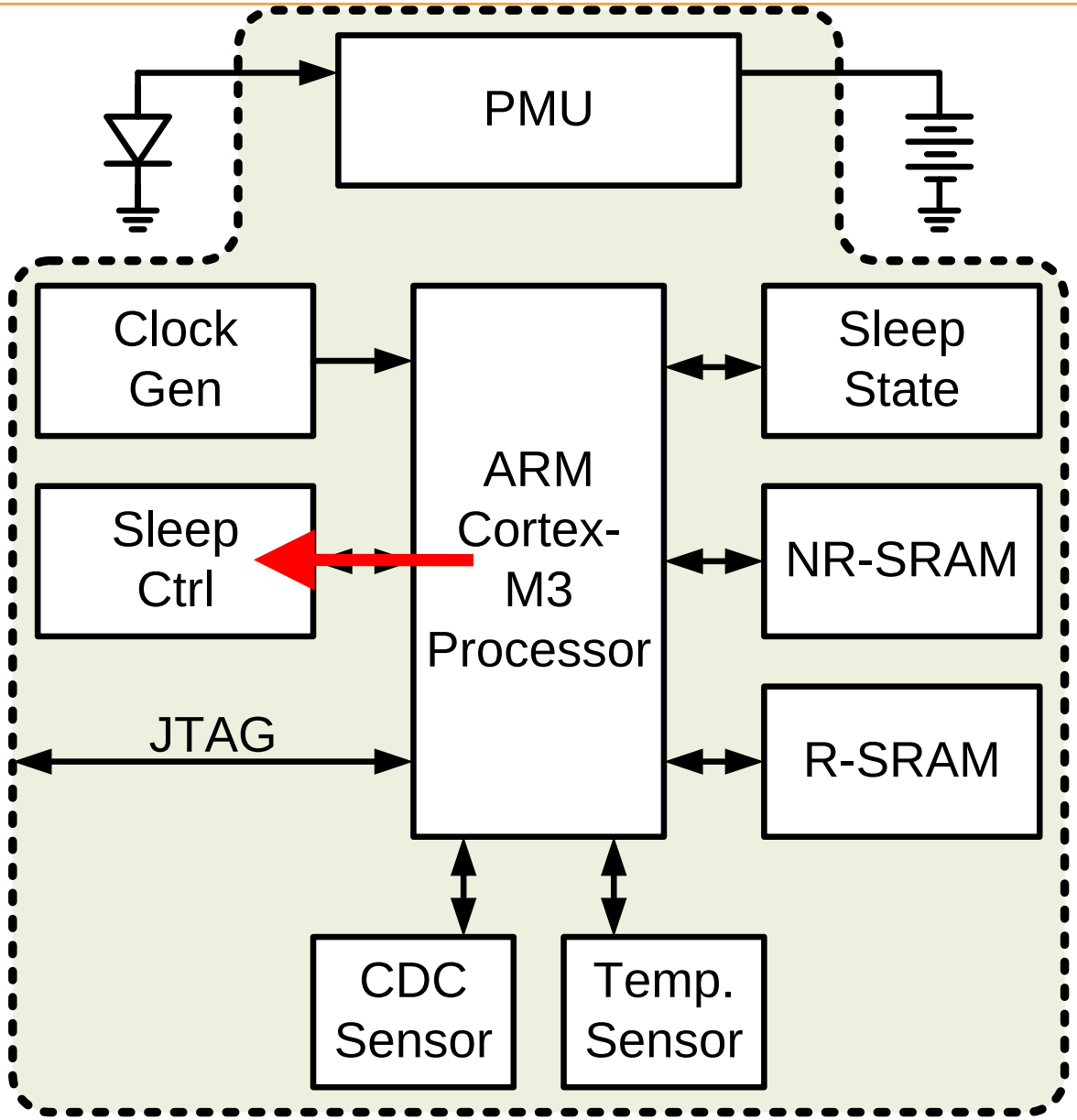

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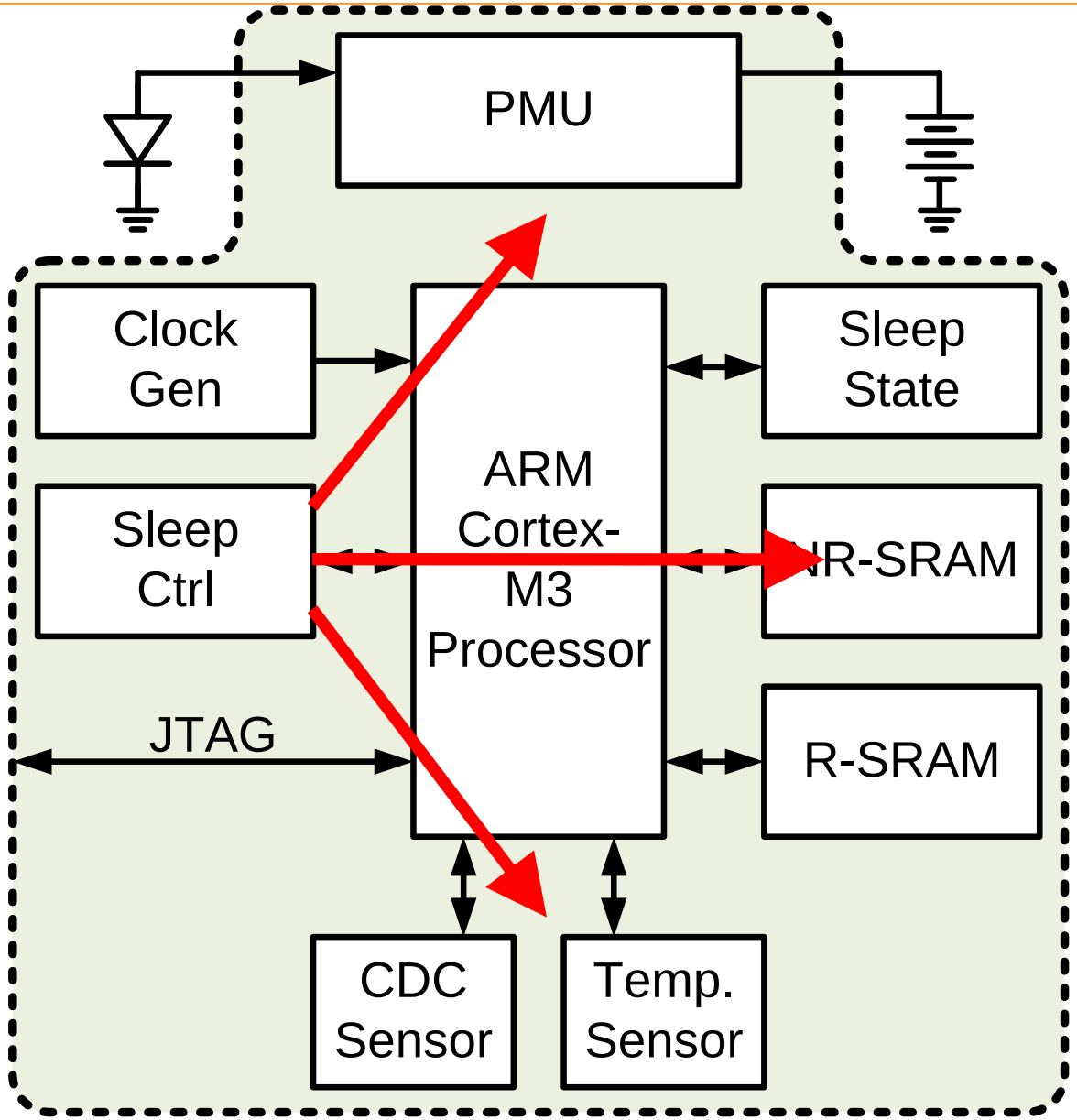

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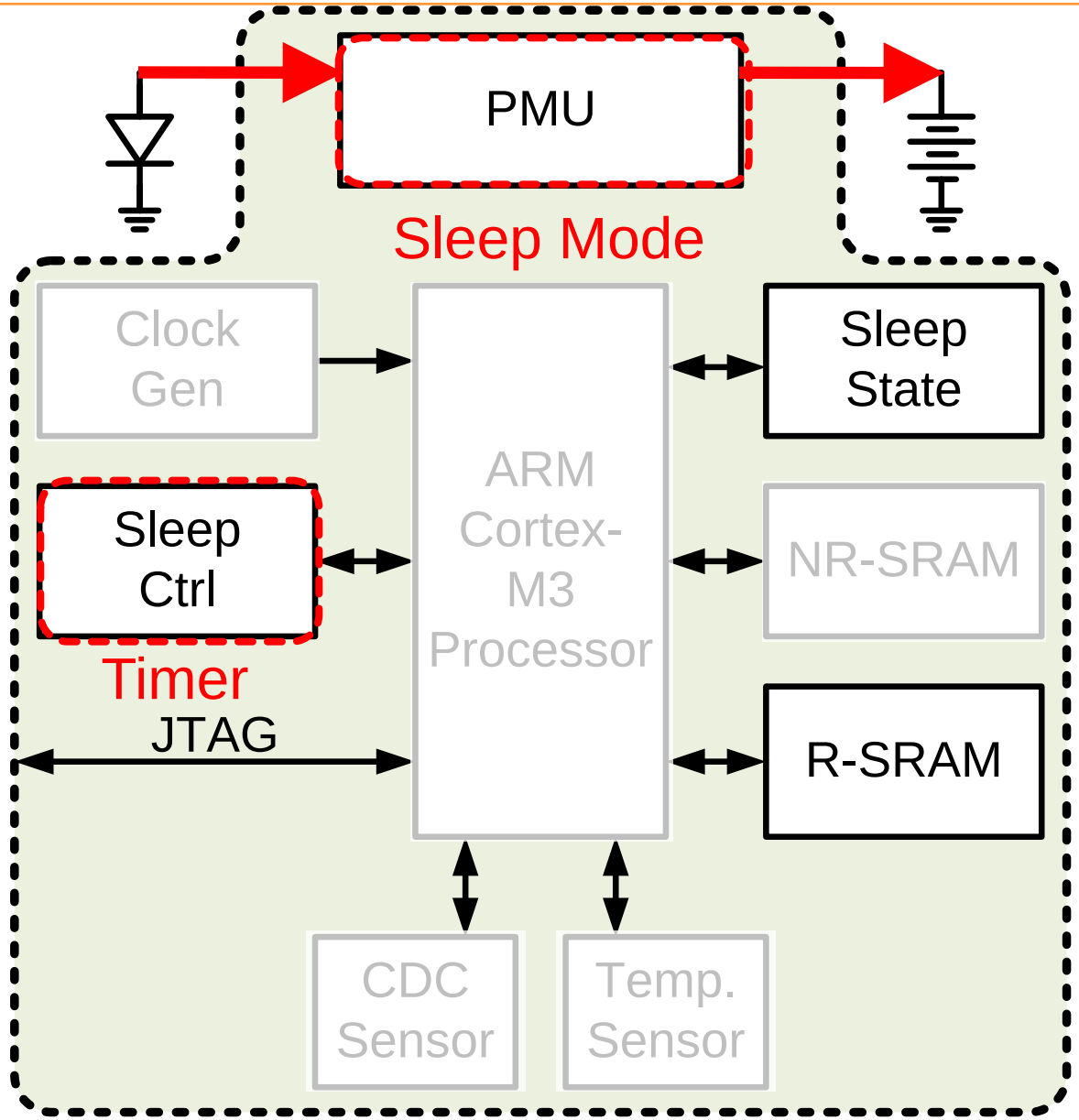

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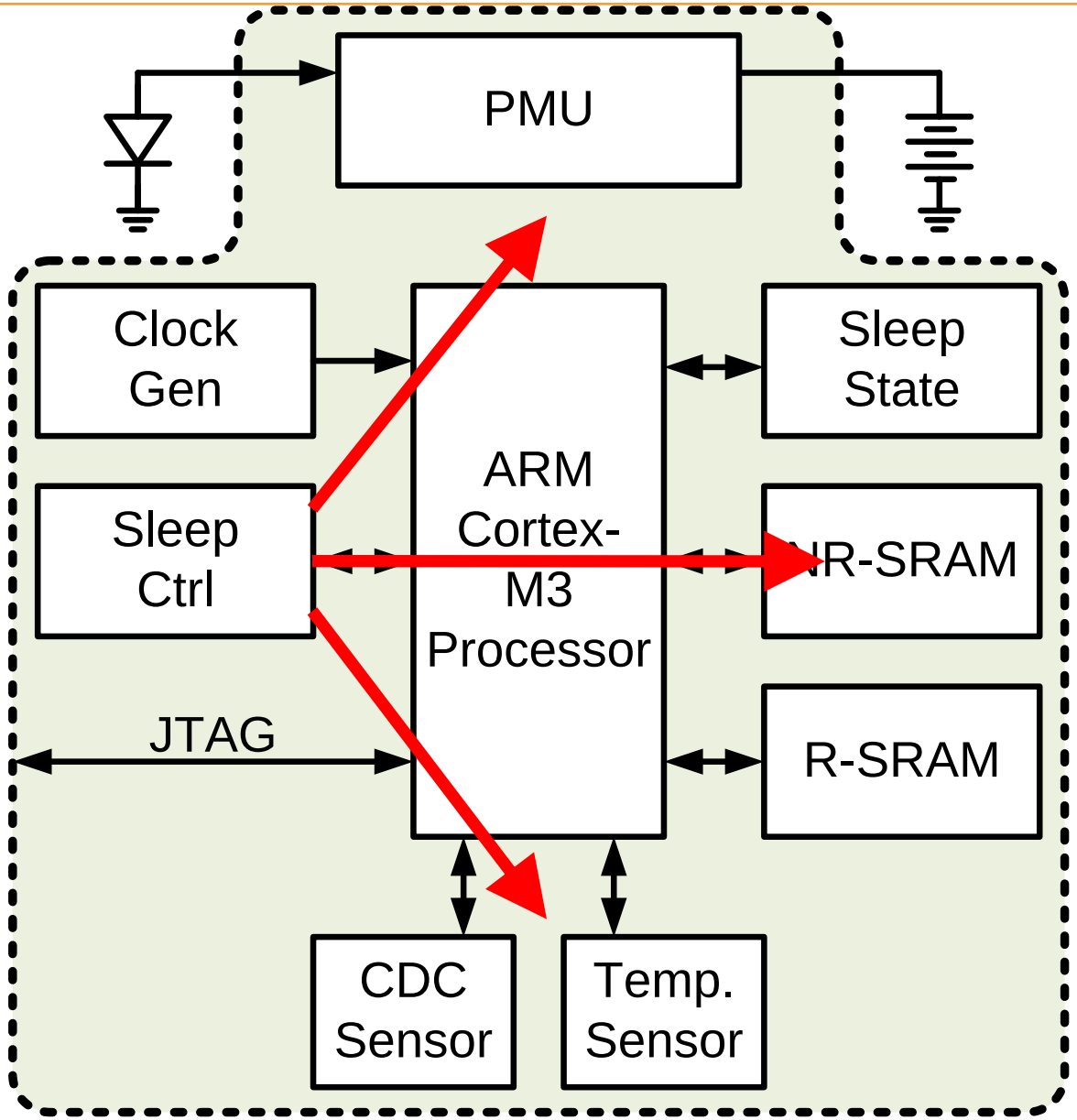

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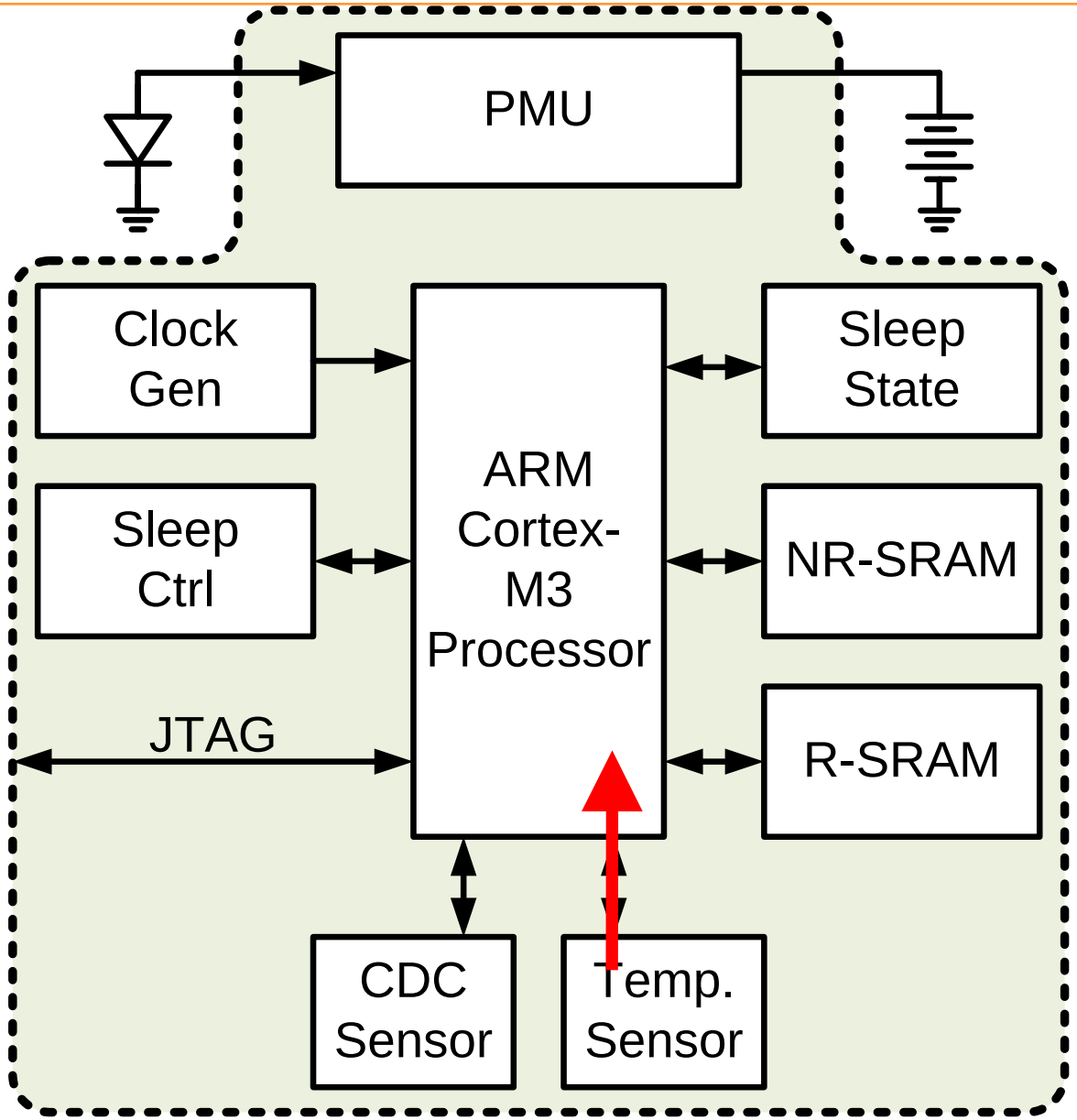
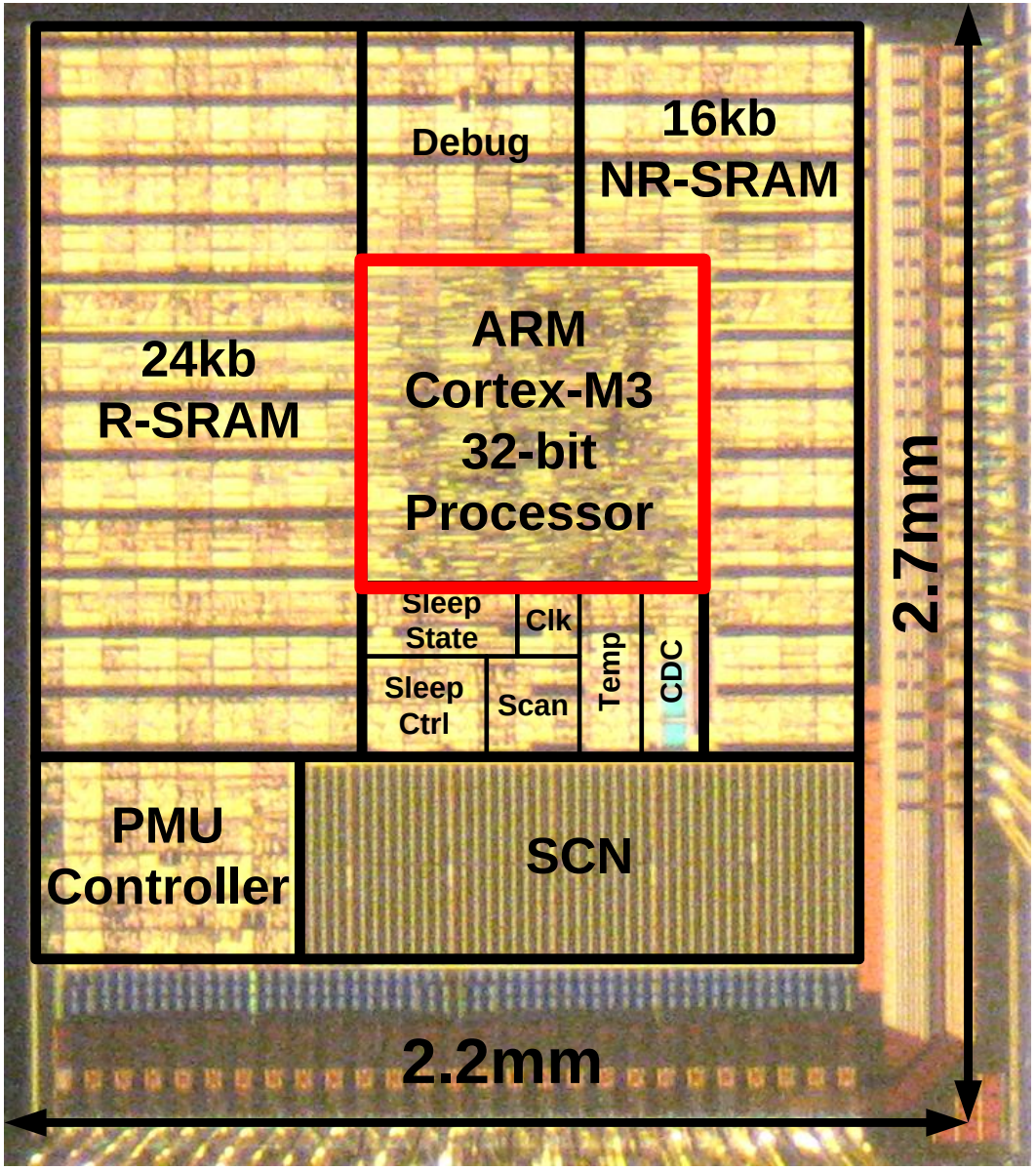


Cortex-M3

- Near-threshold
- 32-bit microcontroller
- 0.18 µm CMOS
- Standard cell library
  - Removed gates with 4+ transistor stacks for robustness
  - Removed gates with size 4x and larger for power/performance tradeoff
  - Characterized at low voltage

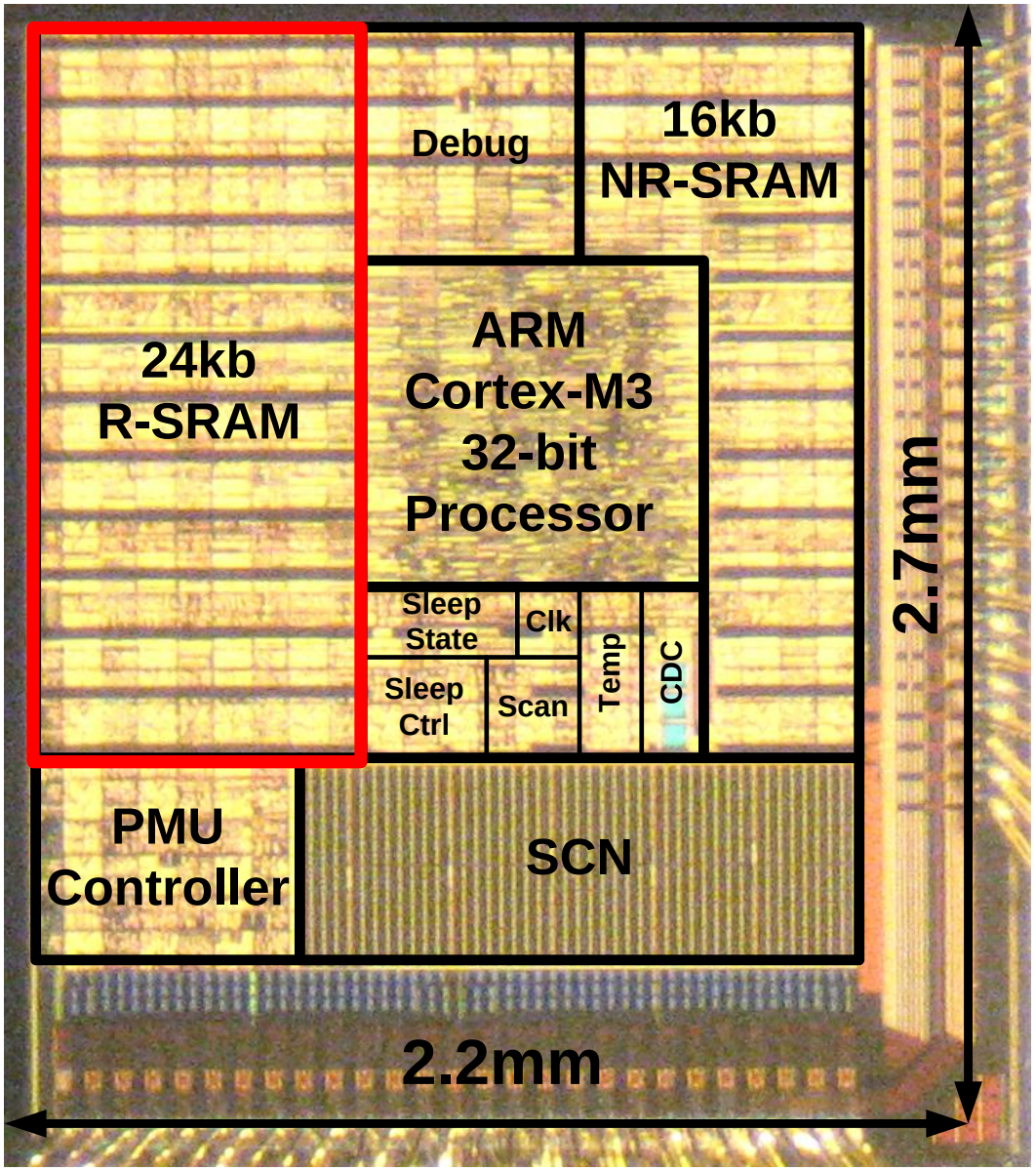


R-SRAM

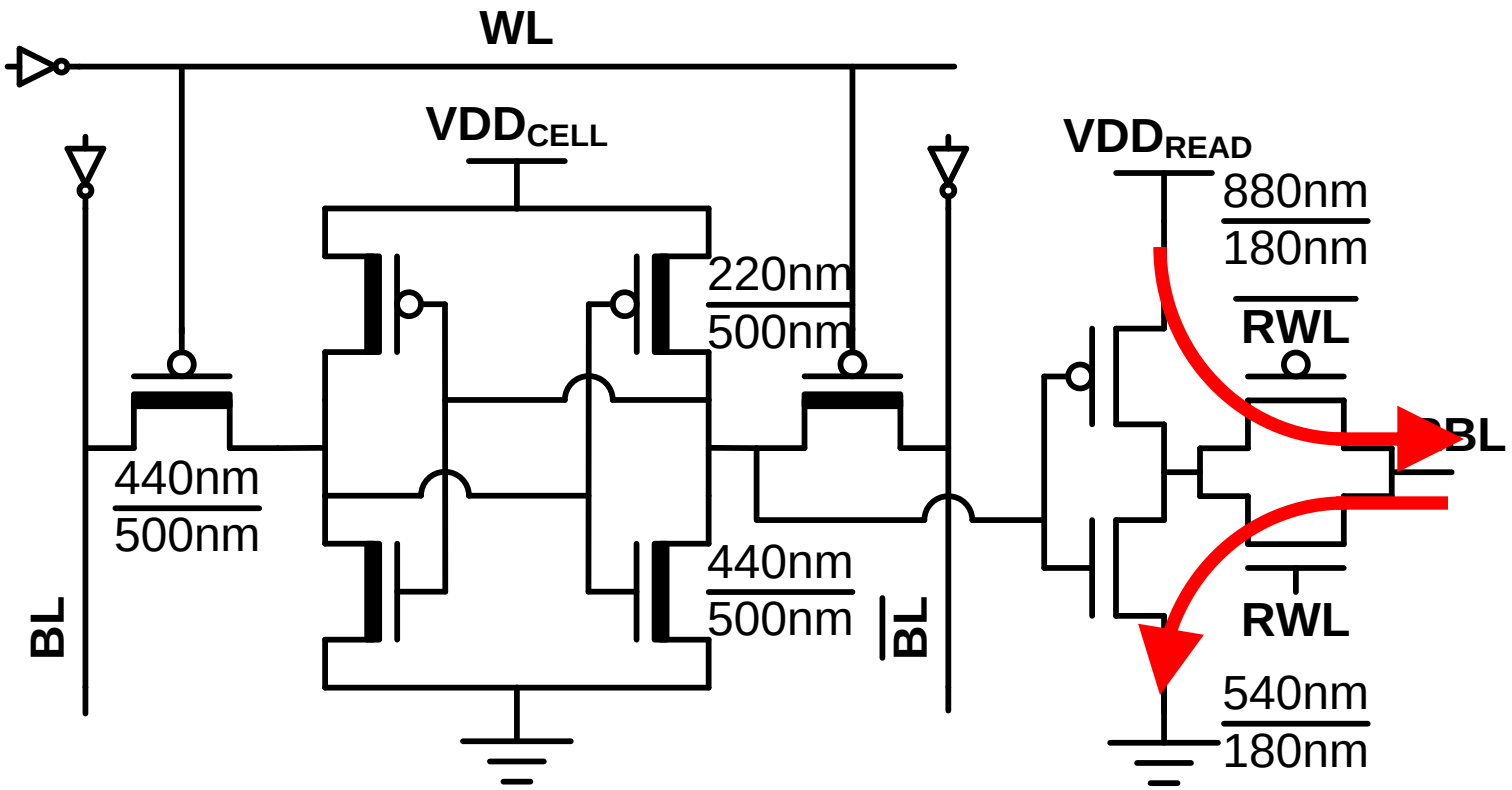
- Instruction memory
- Data logging

- Powered on during sleep
- Low leakage data retention
- Banks can be individually shut down
- Reduce leakage of unused SRAM

- Twelve 2 kb banks

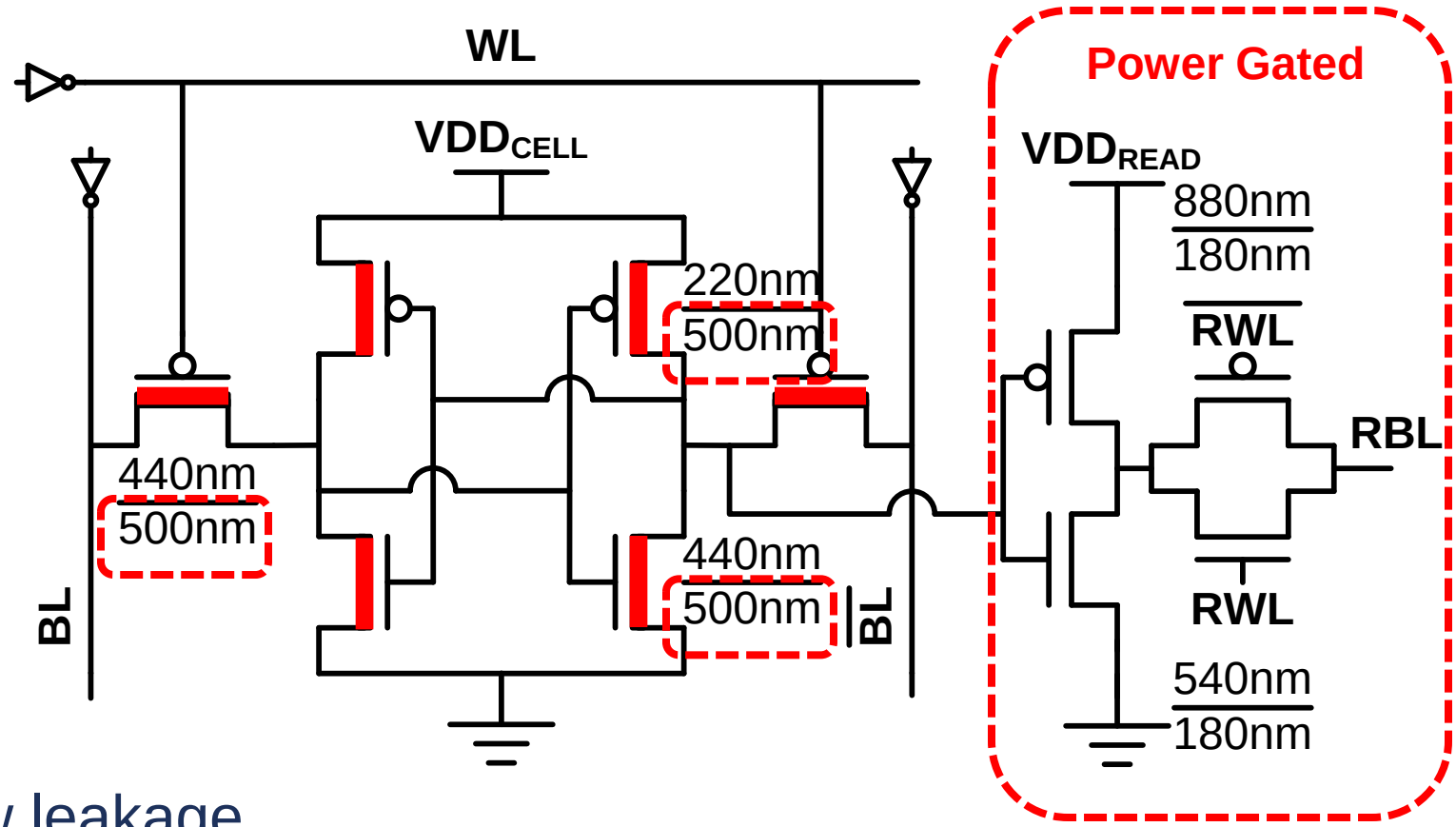


R-SRAM Operation



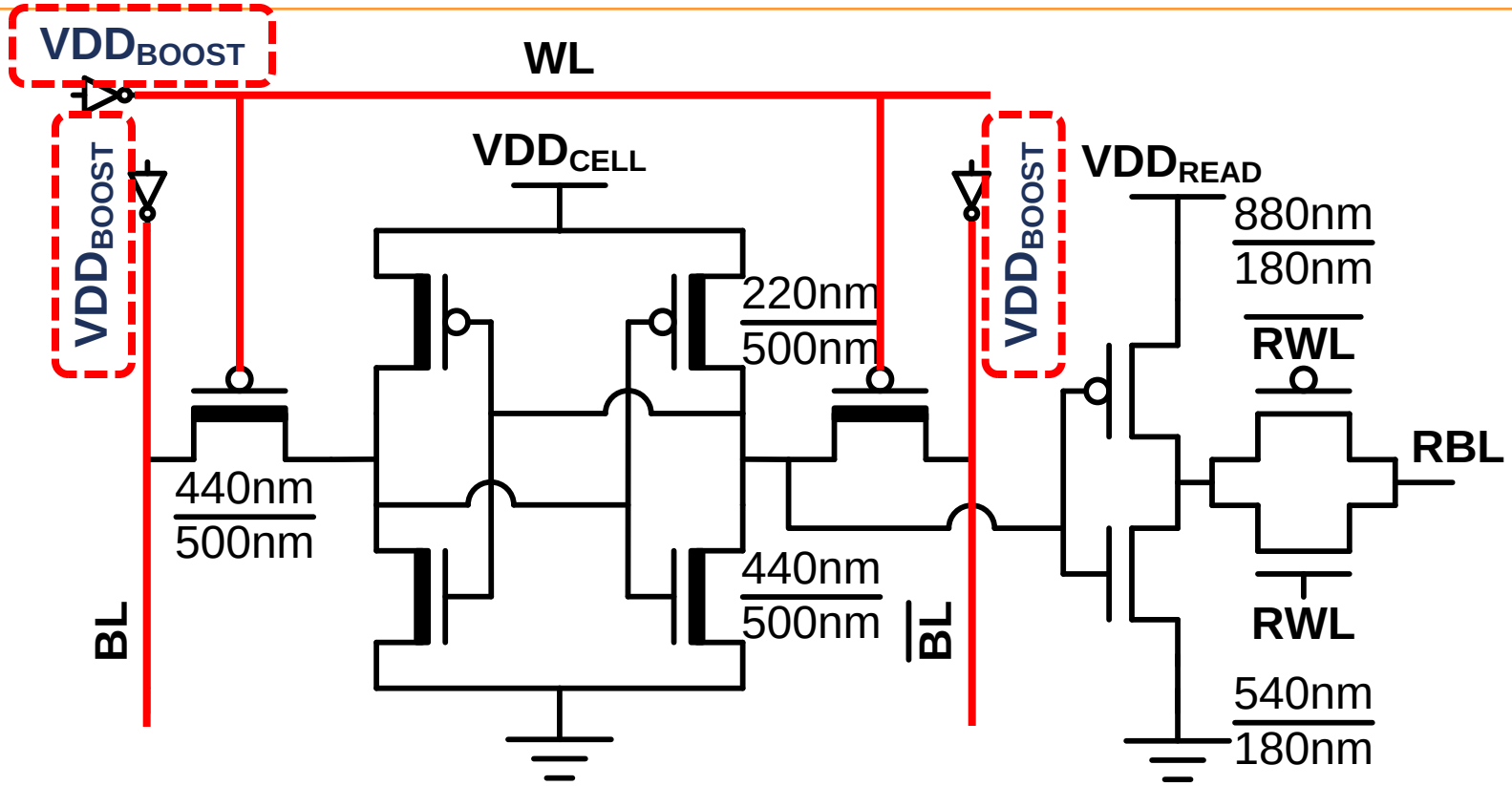
- Robust 400 mV operation
  - Read buffer prevents read upset failures
  - Read buffer pull up prevents unwanted RBL discharge

R-SRAM Operation



- Low leakage
  - 6T portion not power gated to retain data
  - Power gate read buffer during sleep
  - IO devices and length biasing

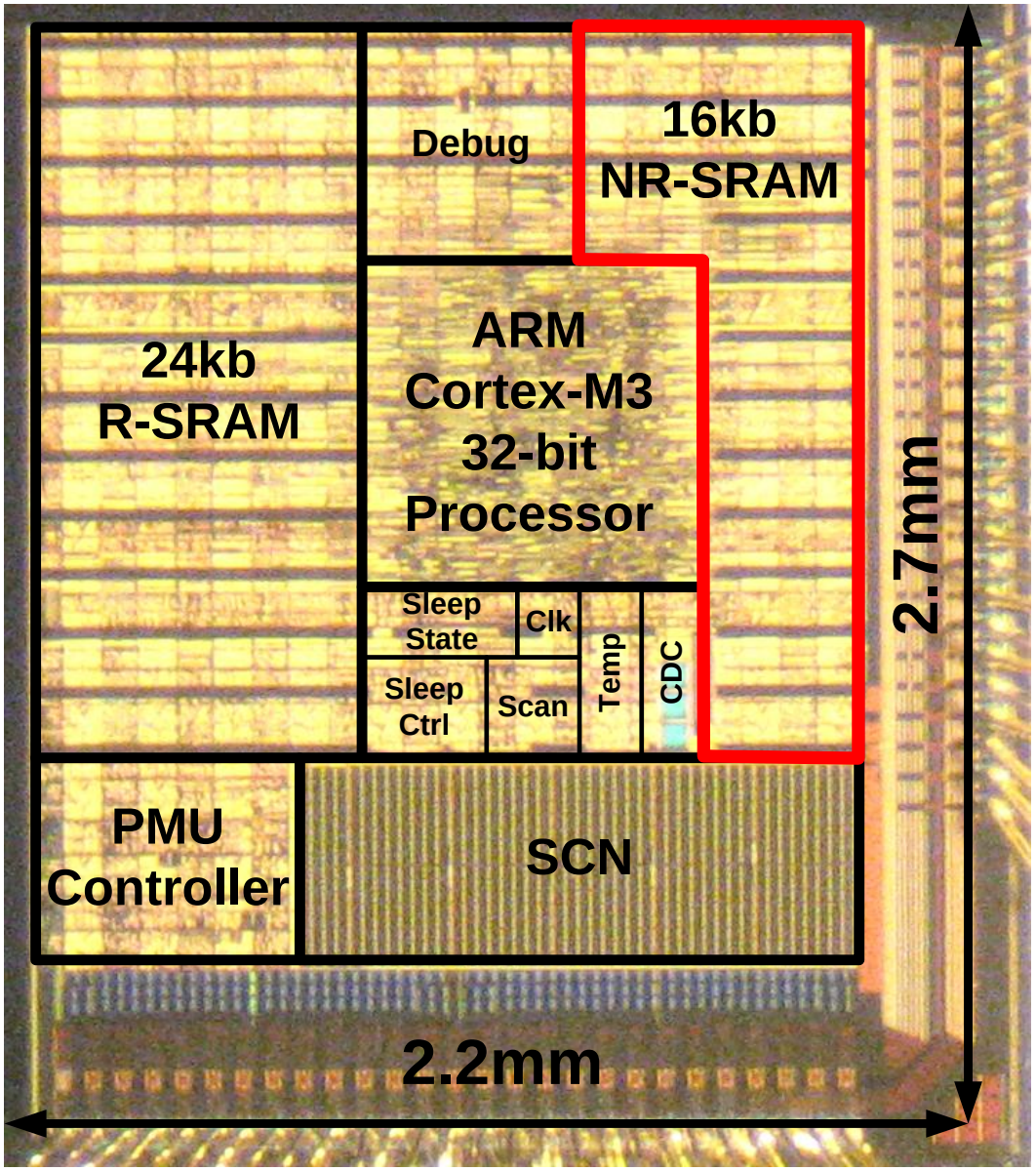
R-SRAM Operation



- Higher speed operation (write limited)
  - HVT PMOS pass gates increase speed by 50%
  - 550 mV VDD_{BOOST} is readily available from the PMU
  - WL and BL boosting increases speed by 2.5x

NR-SRAM

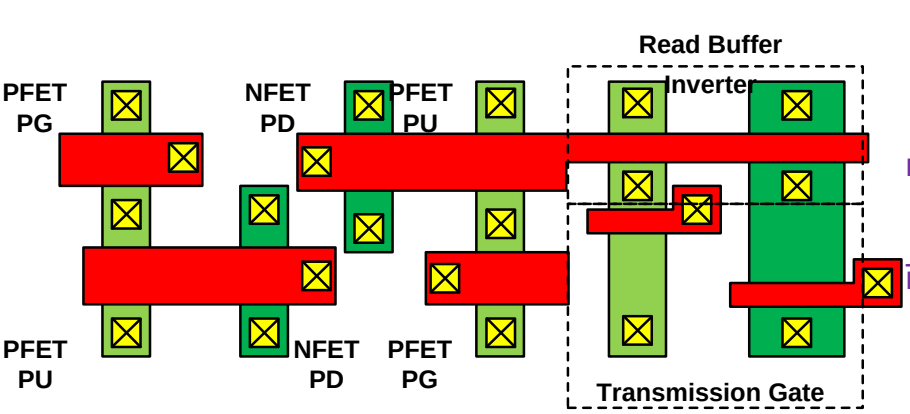
- Temporary storage for DSP algorithms
- Power gated during sleep
- Similar 10T topology to R-SRAM
- All SVT devices
- SVT NMOS pass gates are used for speed
- No pass gate boosting
- Eight 2 kb banks

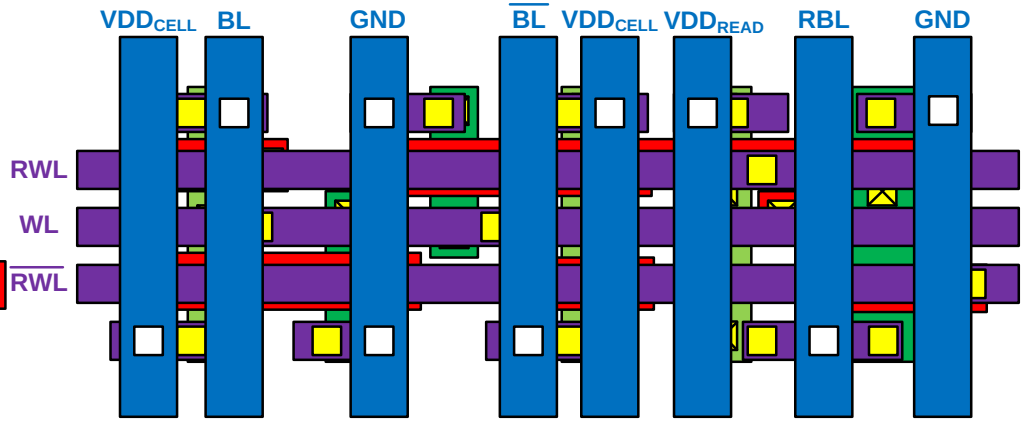


SRAM Summary and Layout

0.18µm CMOS at 500mV	Phoenix JSSC '09	NR-SRAM	R-SRAM
Devices	14T	10T	10T
Bitcell Area	40.0 µm^2	16.3 µm^2	17.5 µm^2
Energy/Access/Bit	0.22 fJ	0.60 fJ	1.18 fJ
Frequency	100 kHz	1 MHz	1 MHz
Write	Asynchronous	1-cycle	Multi-cycle
Read	1-cycle	1-cycle	1-cycle
Leakage/Bit	7.1 fW	6.3 pW	3.3 fW

R-SRAM Layout





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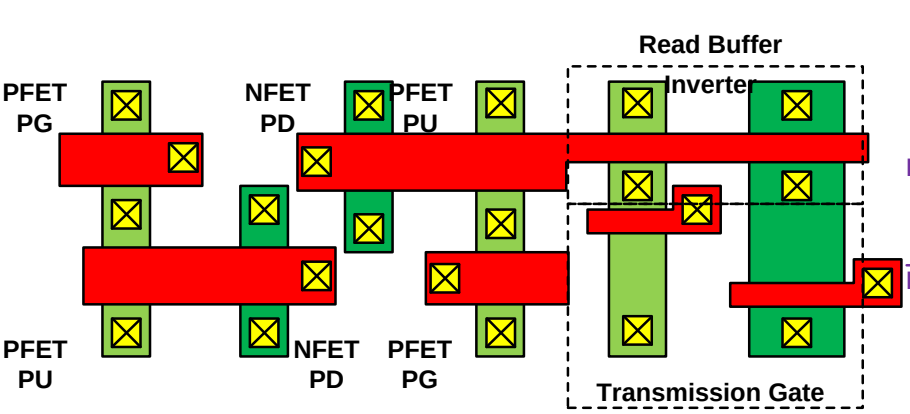
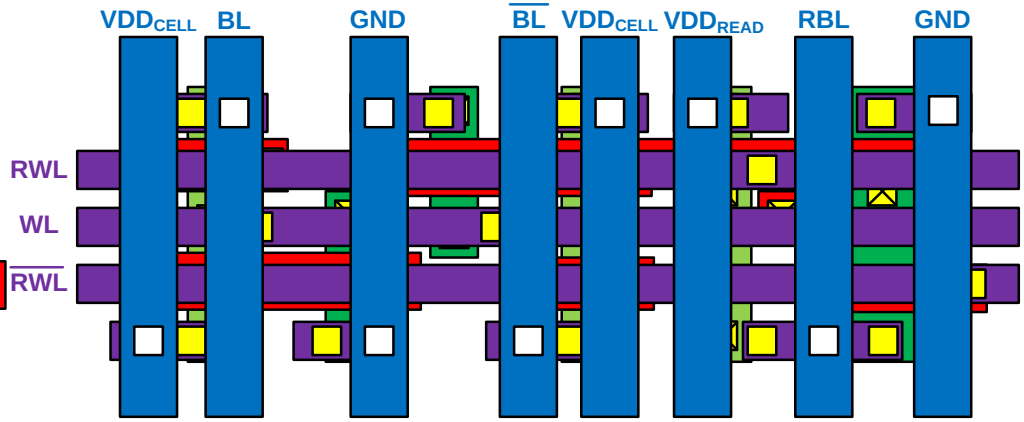
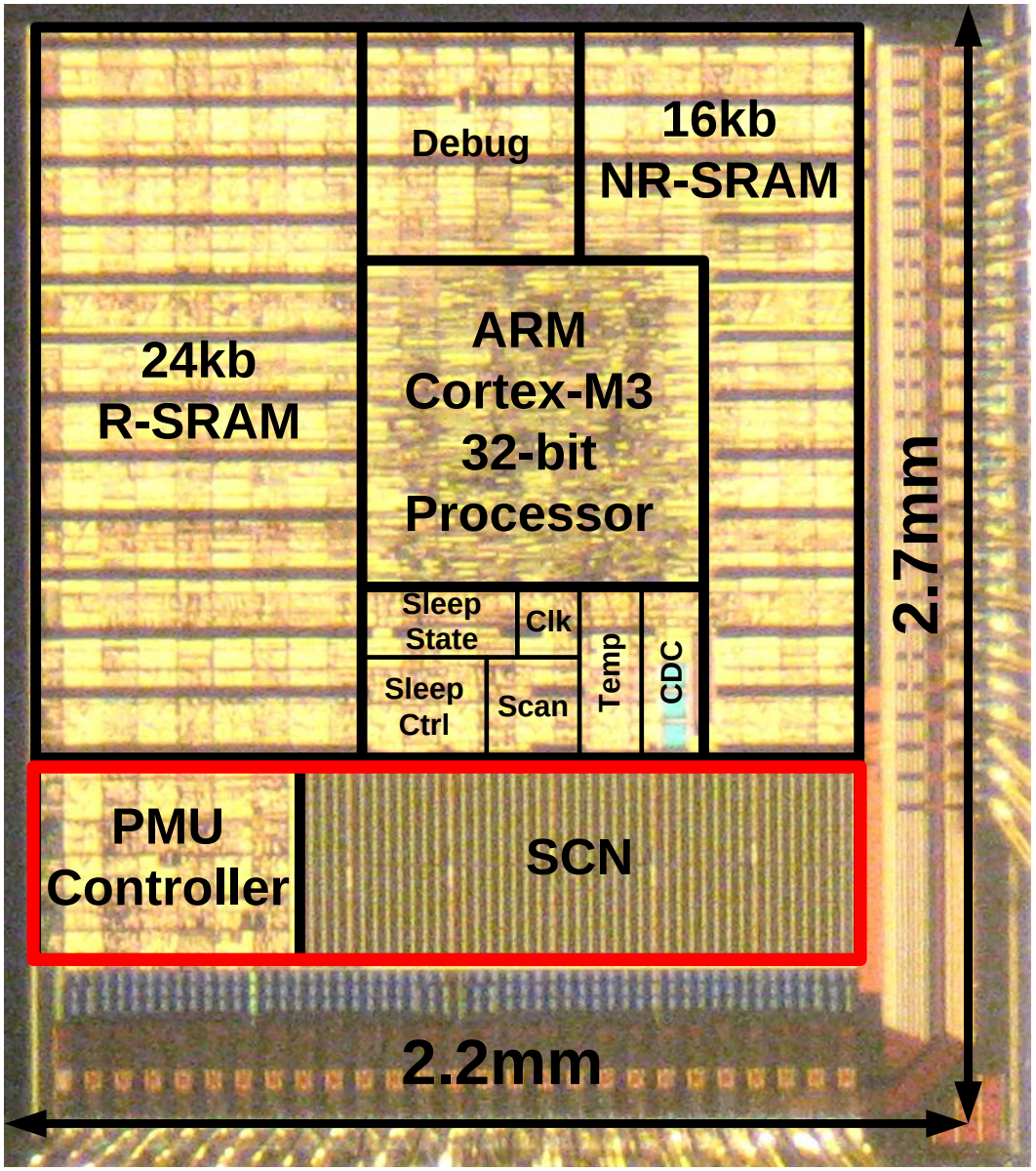


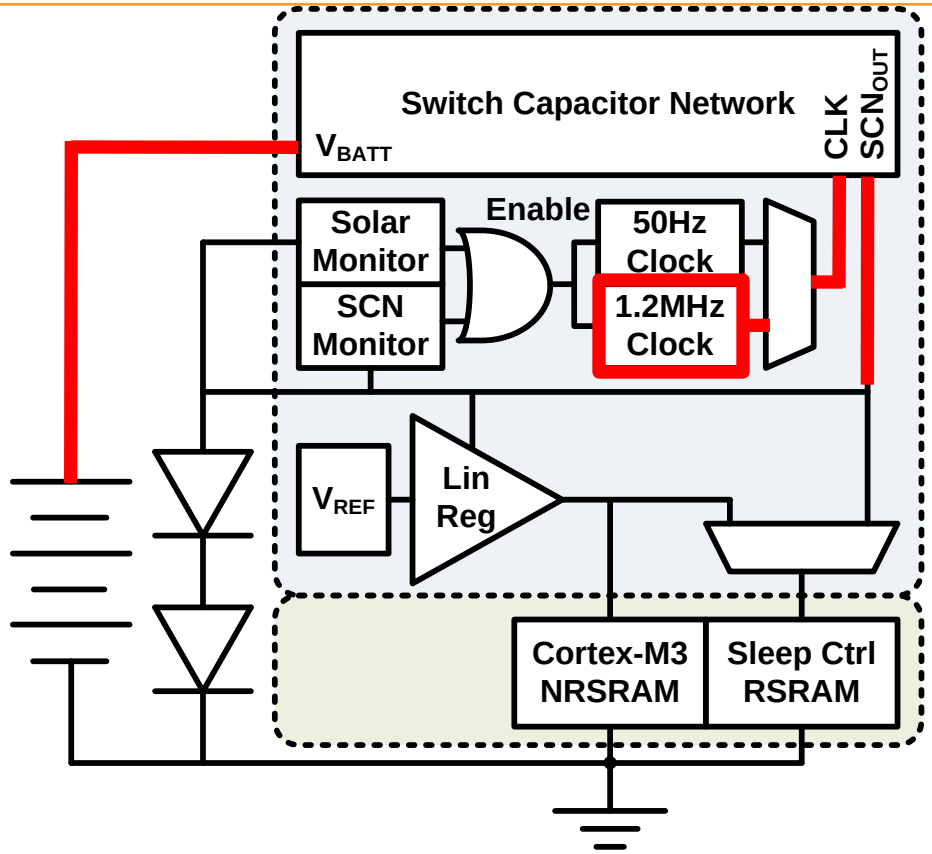


PMU

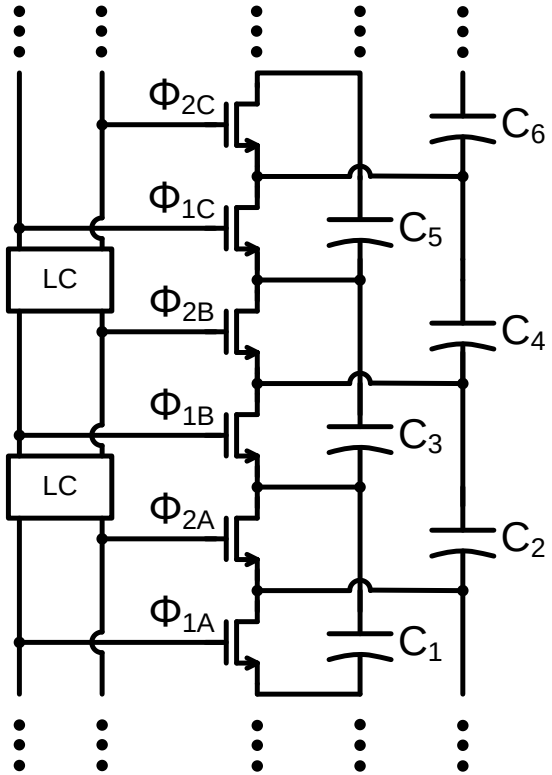
- Converts power among the solar cells, battery and integrated circuits
- Co-optimized for efficiency in active and sleep modes
- Harvests energy during active and sleep mode
- Recharges the battery



PMU Overview – 10µA Active Mode

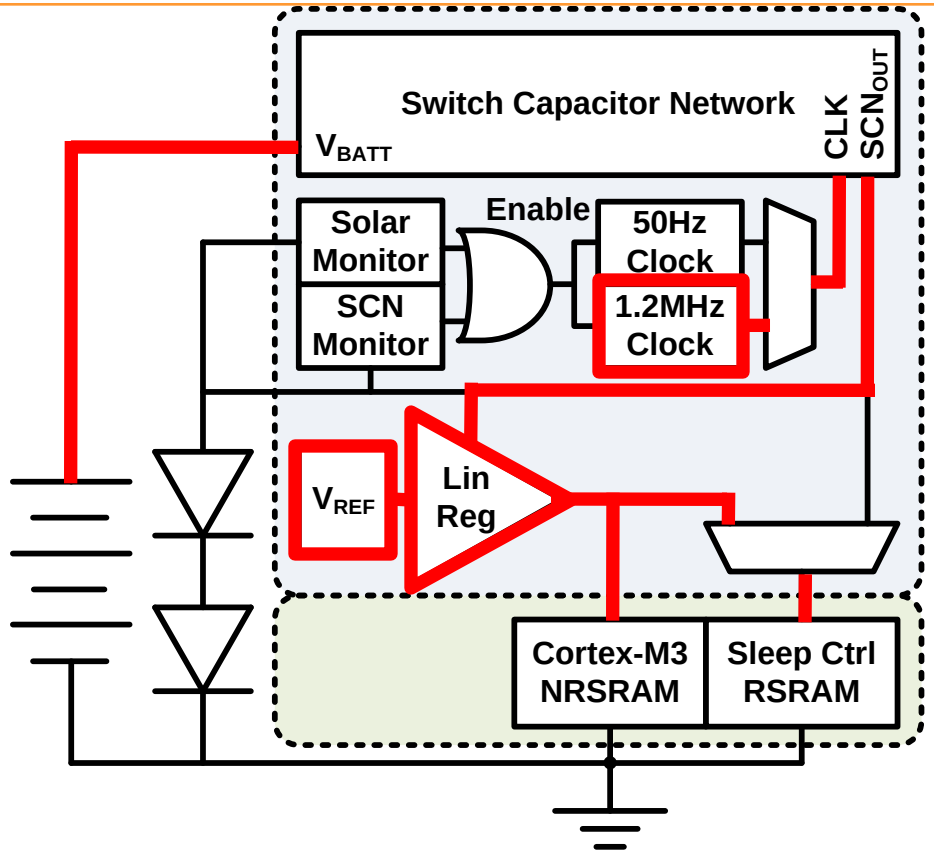


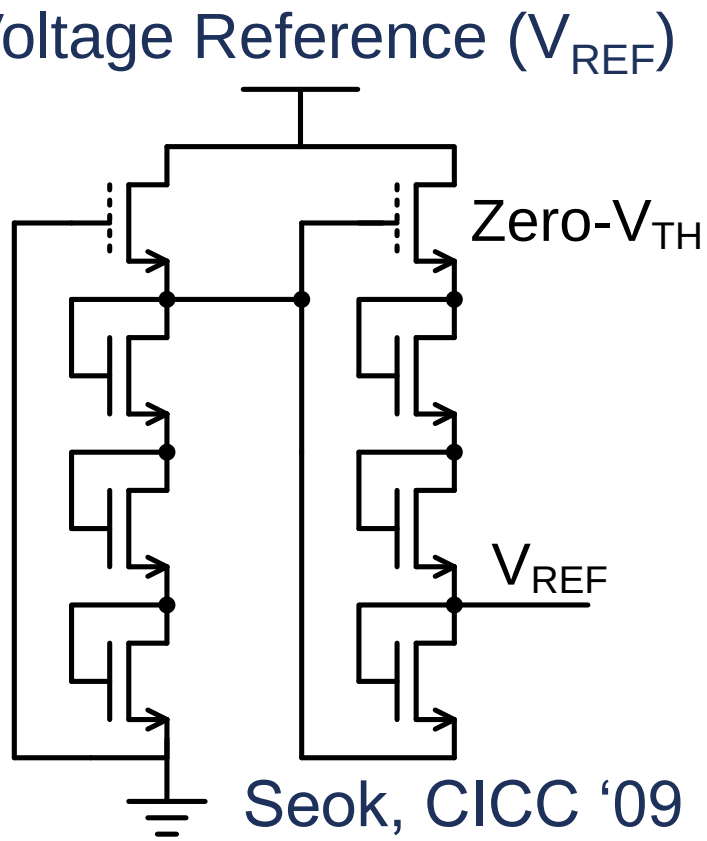
Switched Capacitor Network



- Ladder SCN divides 3.6 V battery voltage by 6
- 1.2 MHz reduced swing clock with level converters
- 8.3x energy reduction over full-swing clocking

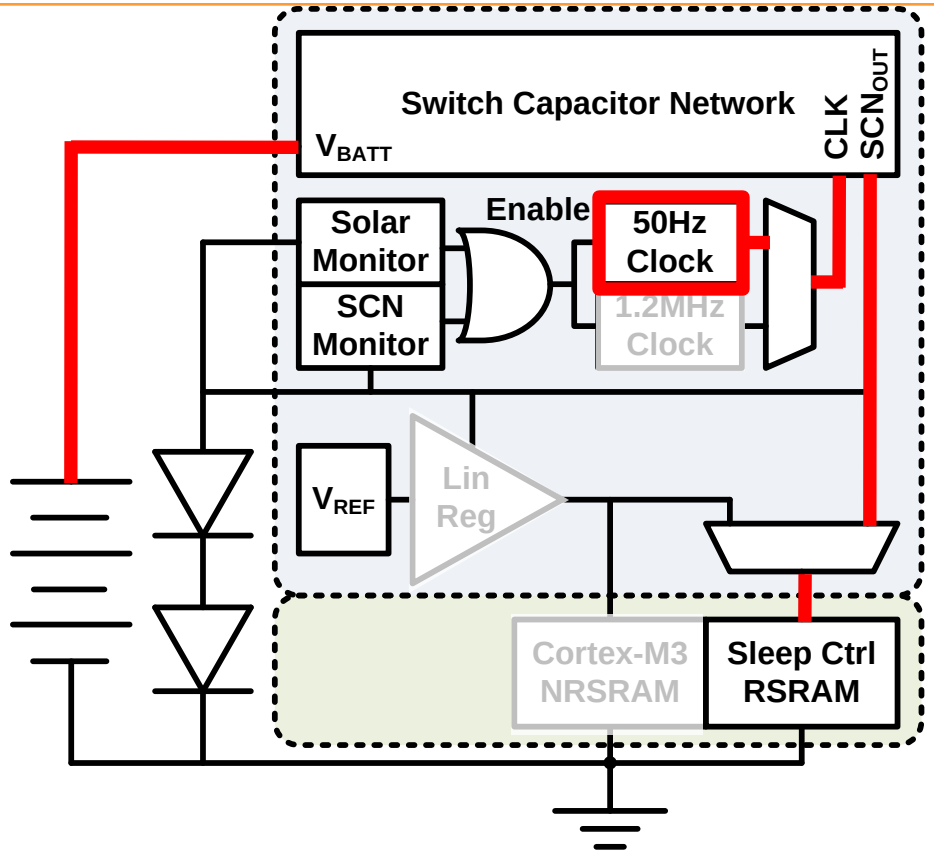
PMU Overview – 10µA Active Mode

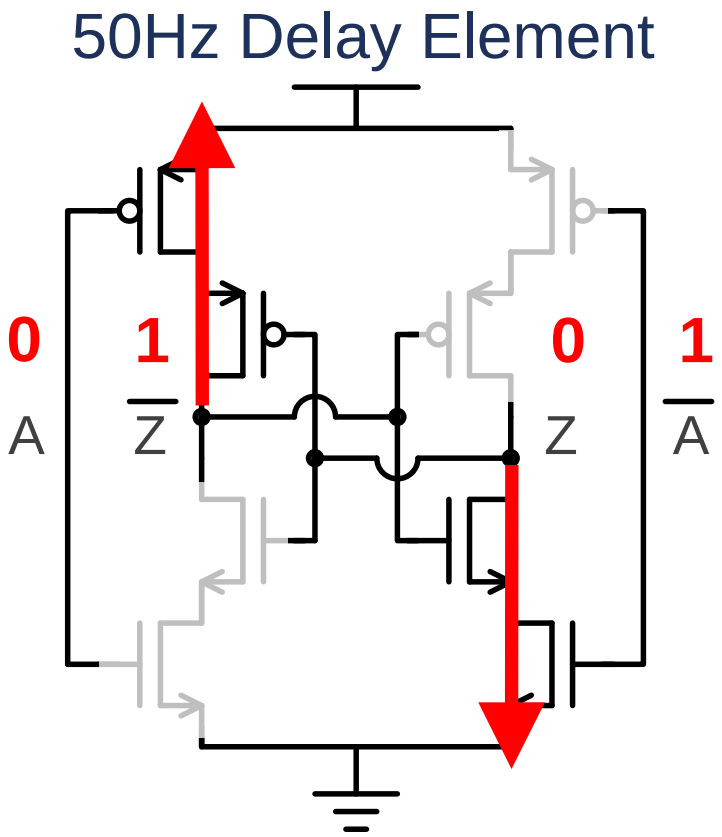




- Sub-V_{TH}-biased linear regulator removes power supply noise
- V_{DD} for Cortex-M3 and SRAM set by 8 pA V_{TH}-based V_{REF}
- 0.05%/V line sensitivity
- 20 ppm/ºC temperature coefficient

PMU Overview – 1nA Sleep Mode





- SCN clocked at 50 Hz
- Linear regulator bypassed and bias current removed
- 63 pW clock generated with leakage-based delay element

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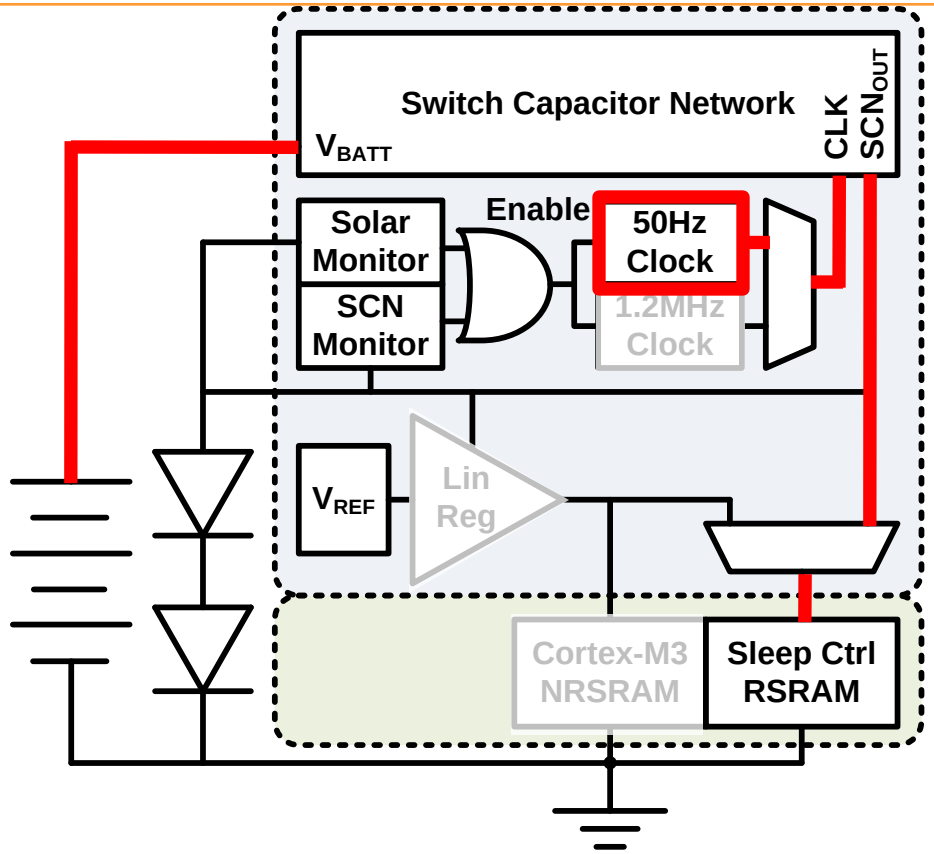
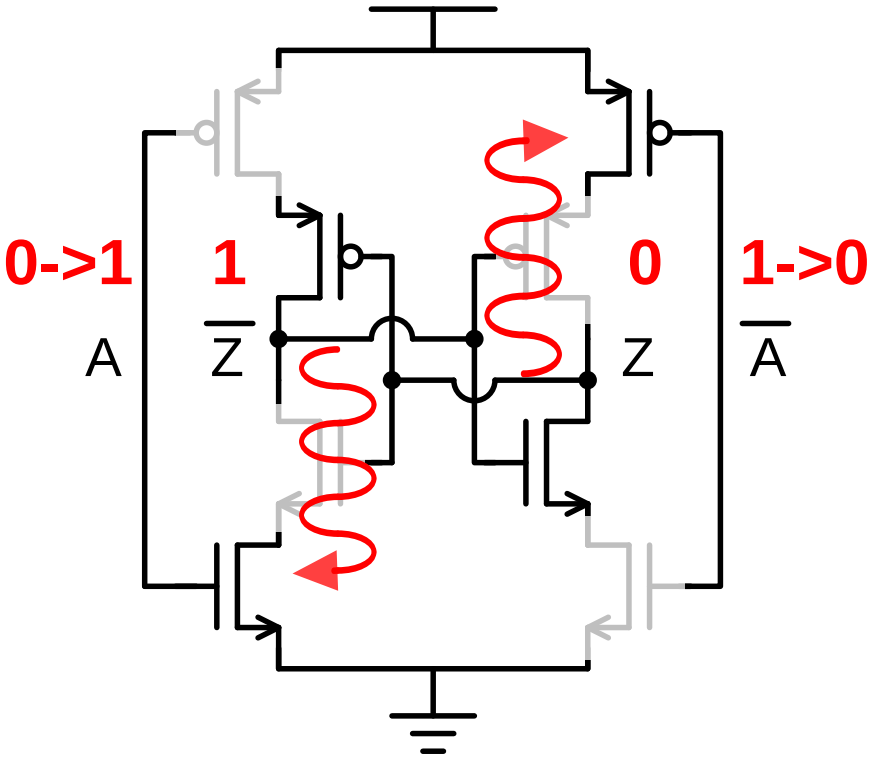


50Hz Delay Element



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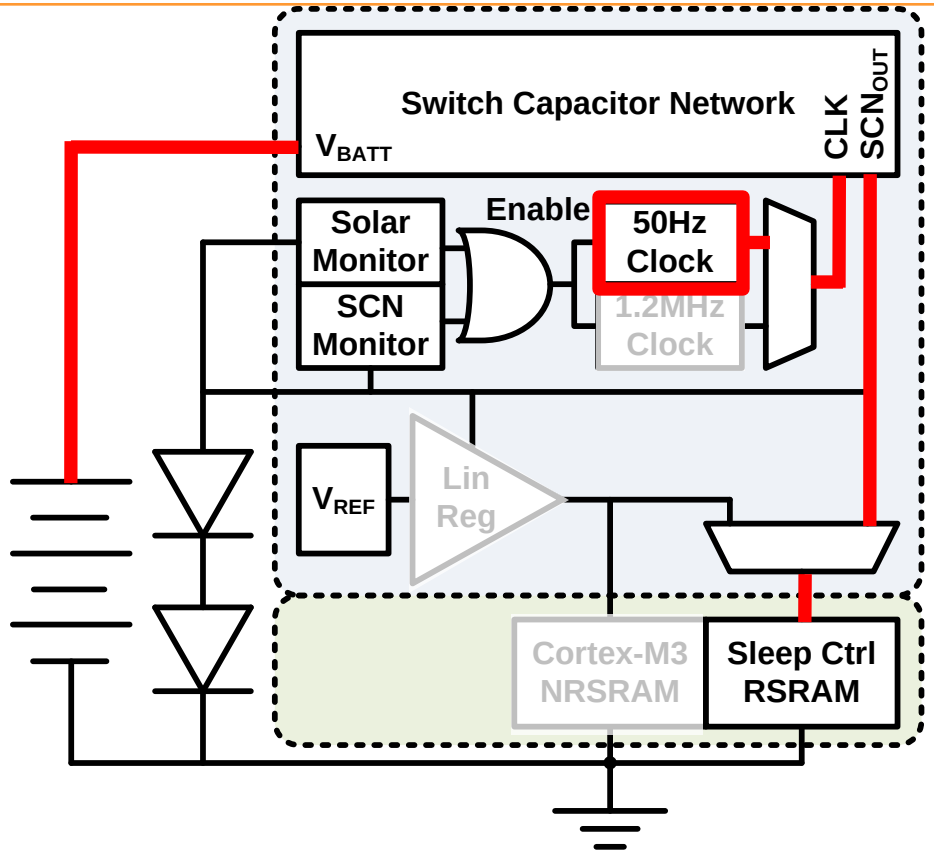

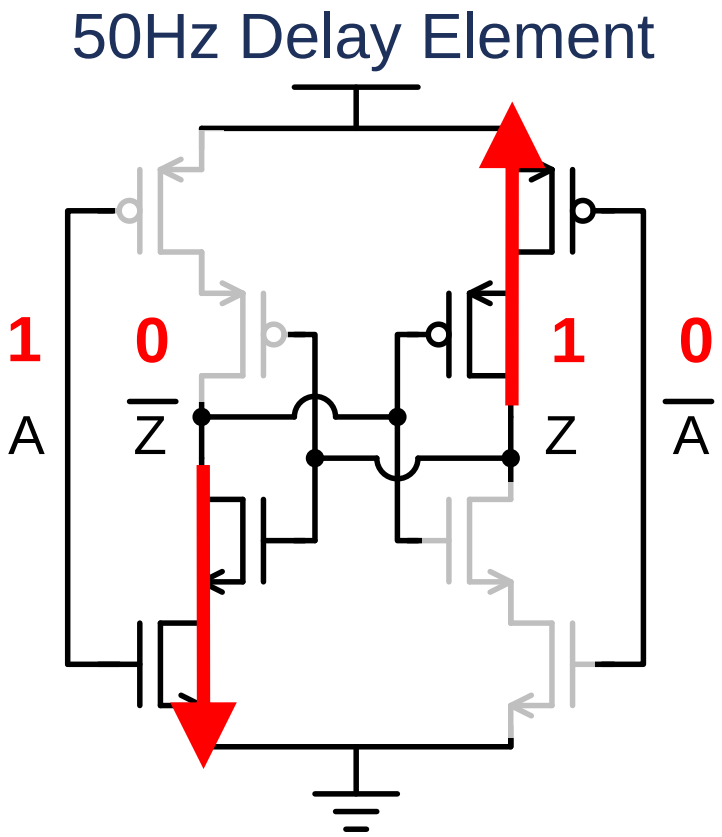

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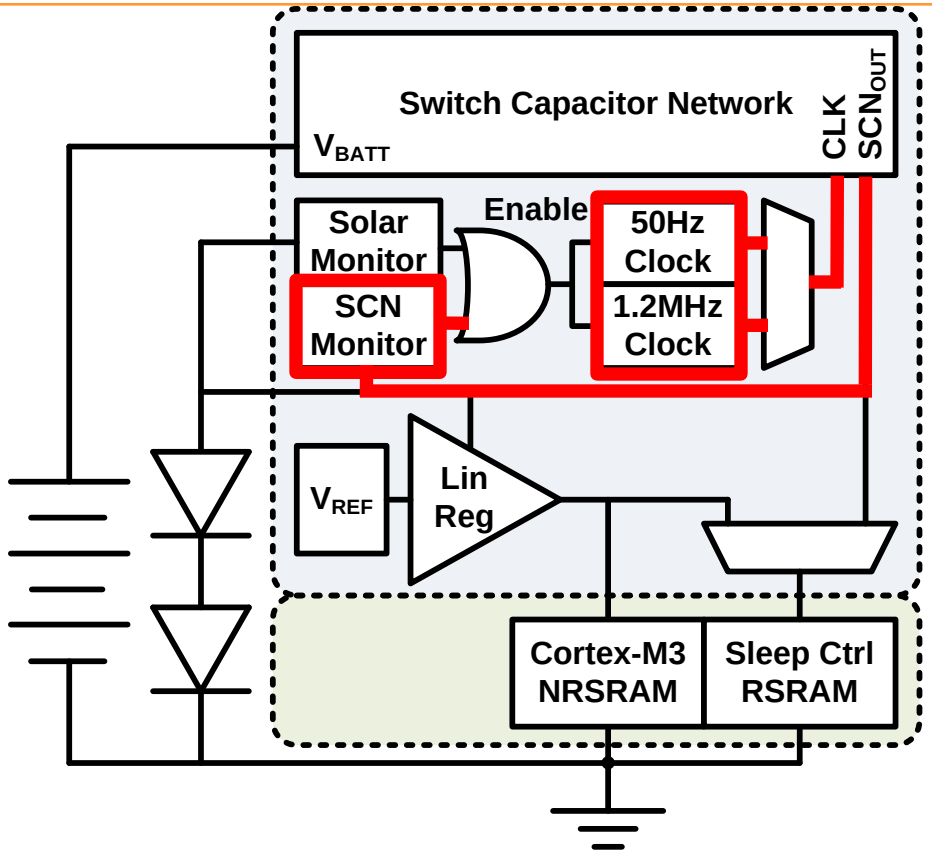
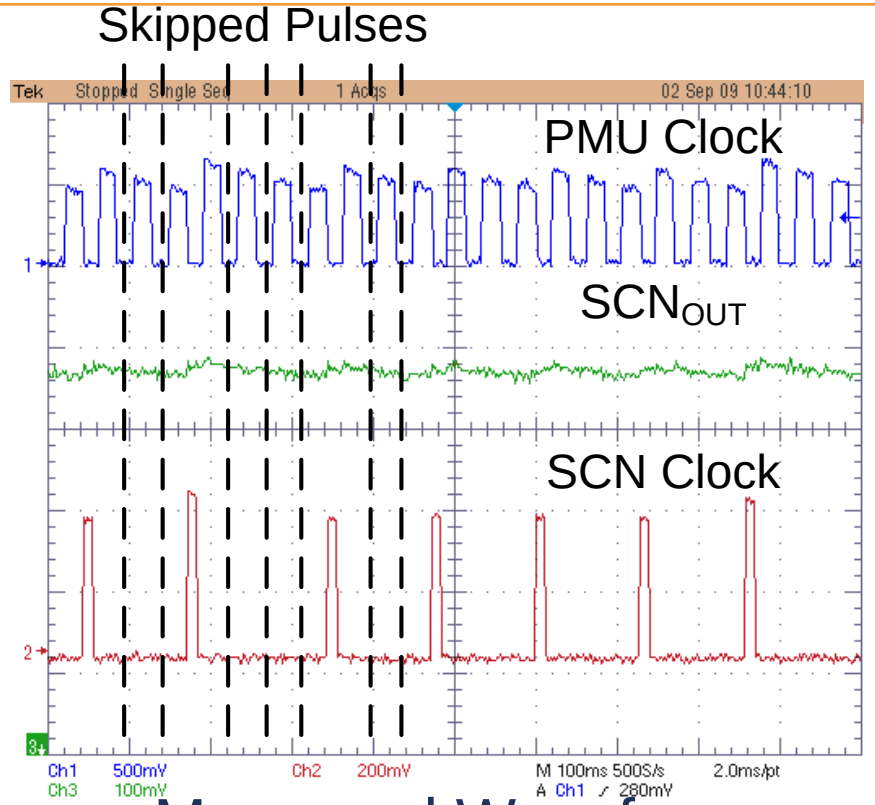
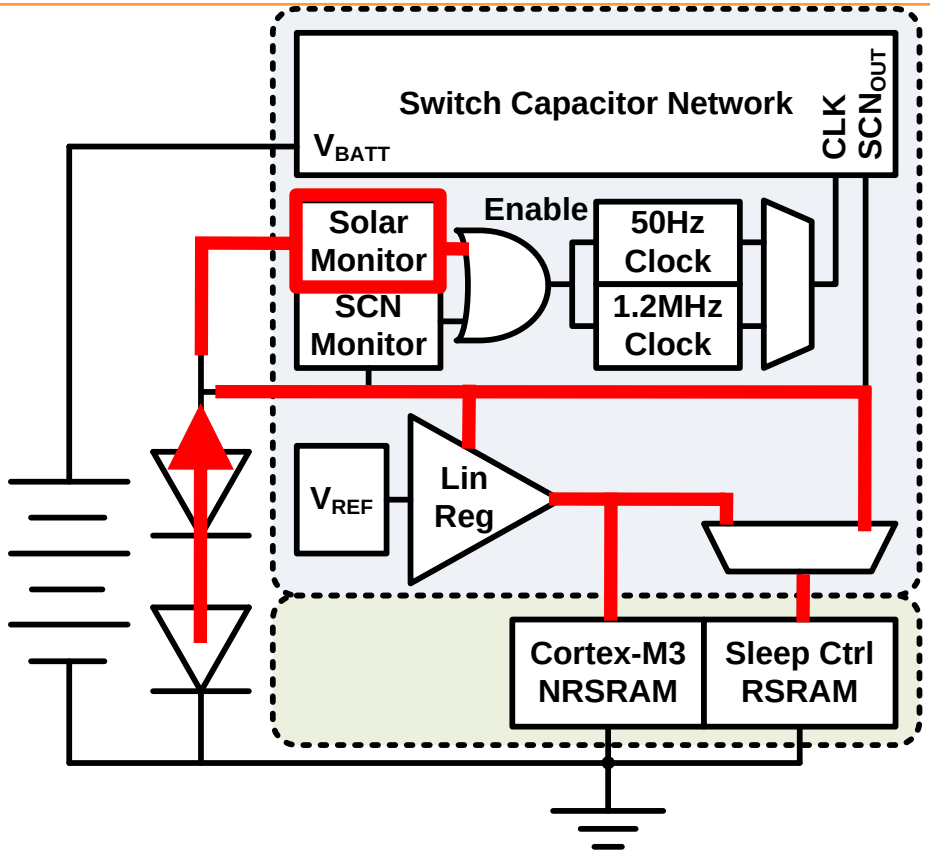
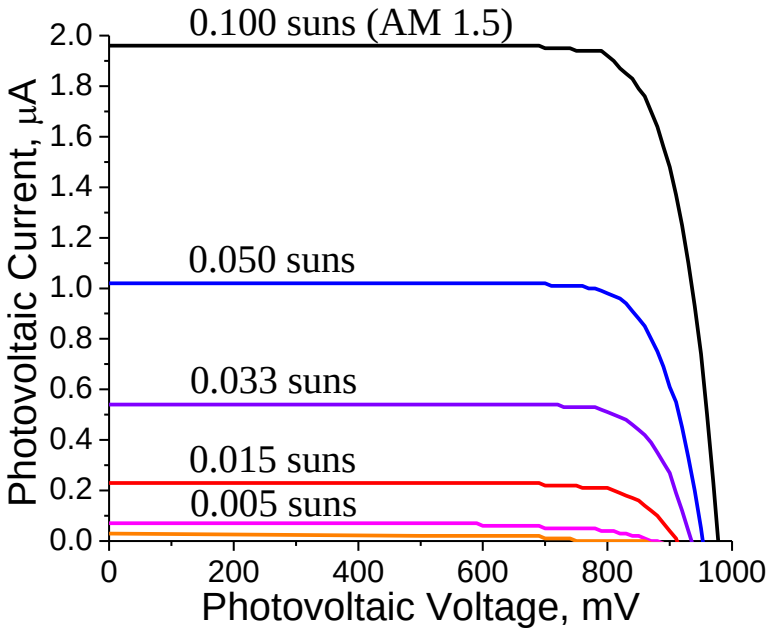




- SCN is clocked on demand to accommodate varying loads
- SCN monitor checks SCN_{OUT} voltage and gates clock
- Reduces clock energy to increase efficiency by 20%

PMU Overview – Energy harvesting





- The solar monitor checks the PV voltage (V_{PV})
- If $V_{PV} > V_{SCNOUT}$, the PV cells are connected to SCN_{OUT}

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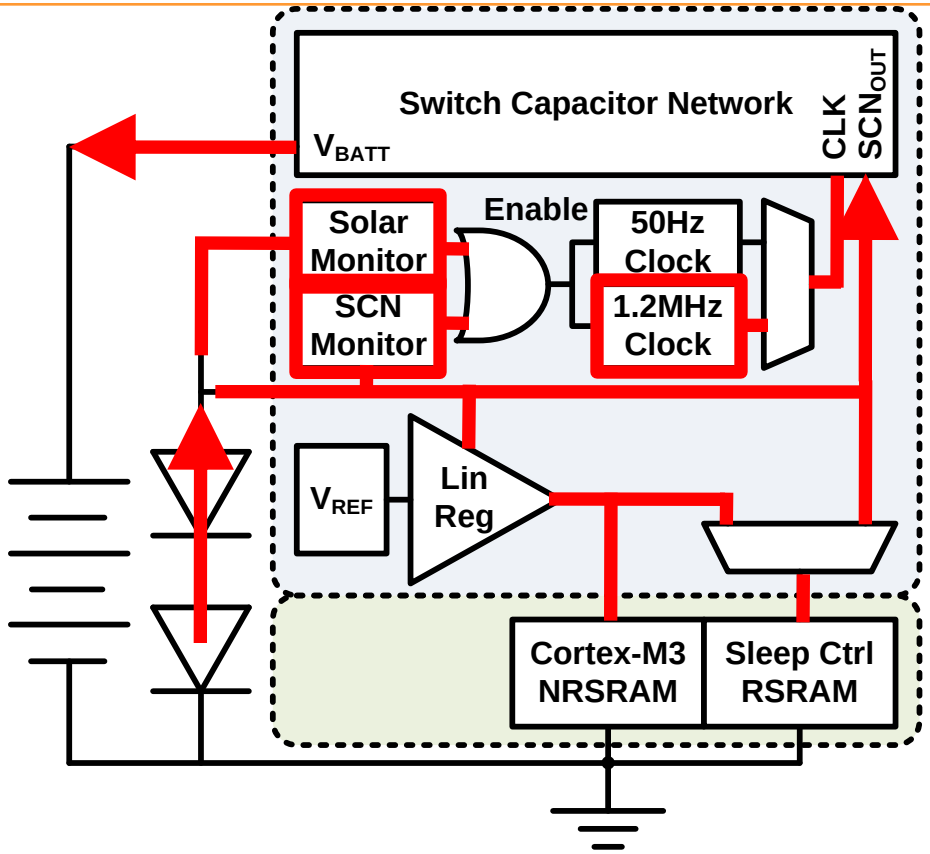
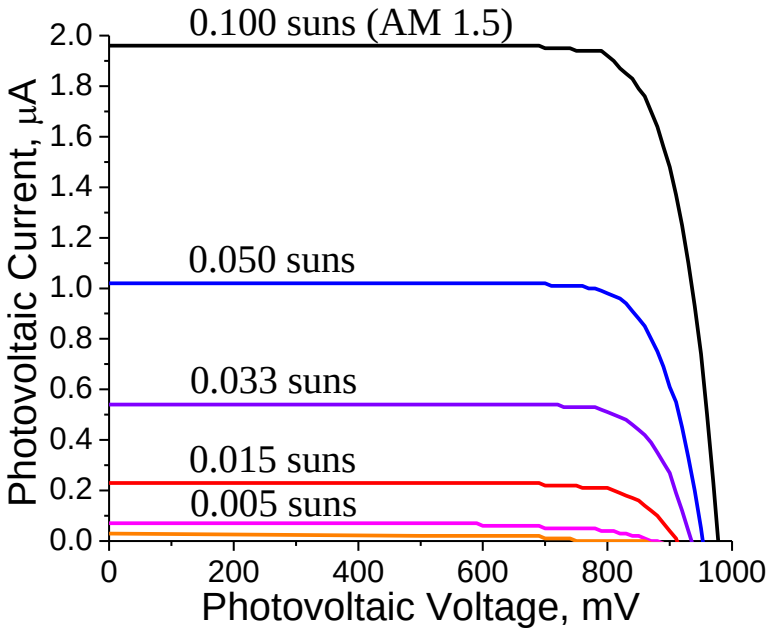
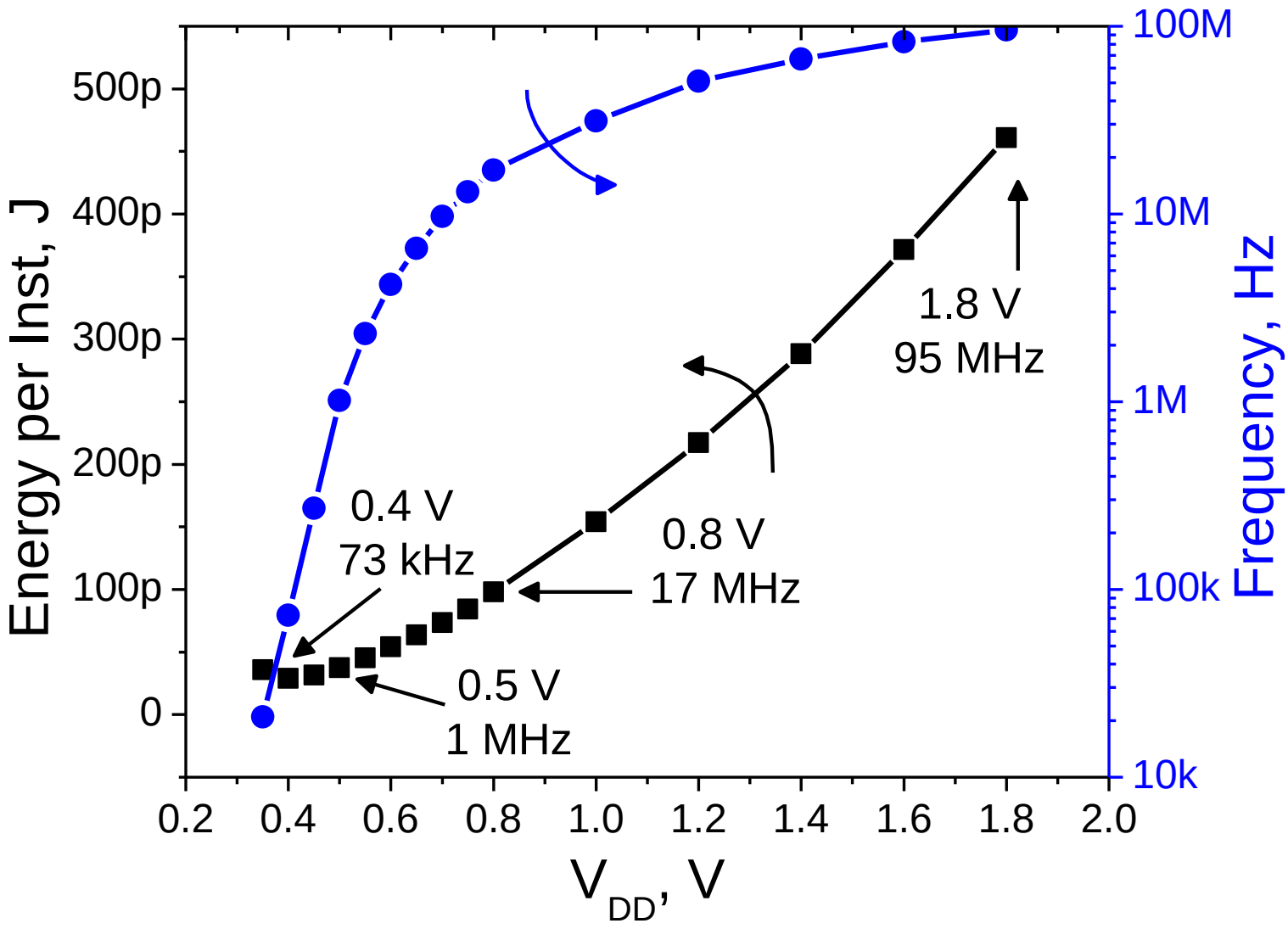




- The solar monitor checks the PV voltage (V_{PV})
- If $V_{PV} > V_{SCNOUT}$, the PV cells are connected to SCN_{OUT}
- If $V_{SCNOUT} > V_{BATT}/6$, the same SCN recharges the battery

Processor Performance vs. Energy



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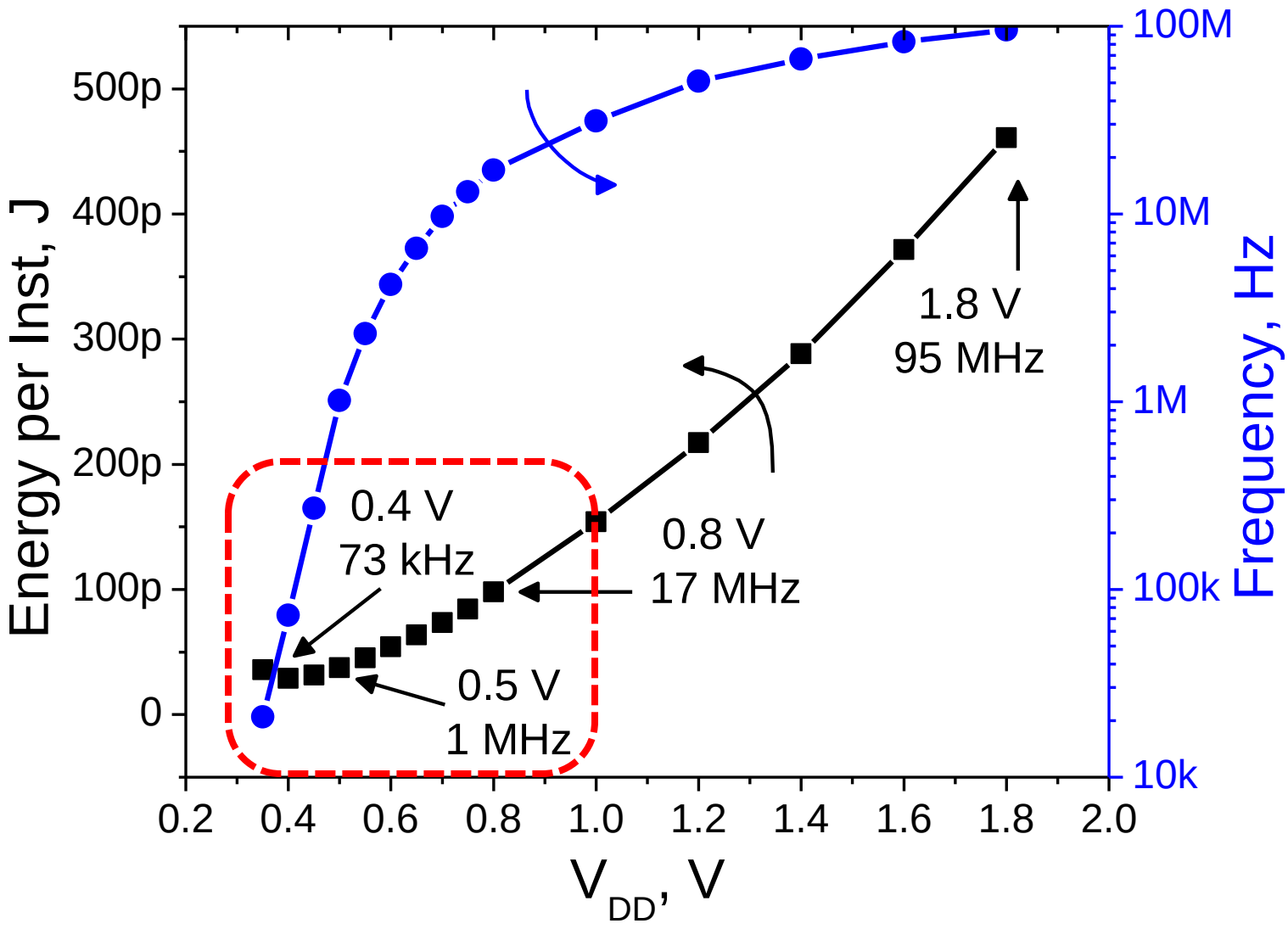
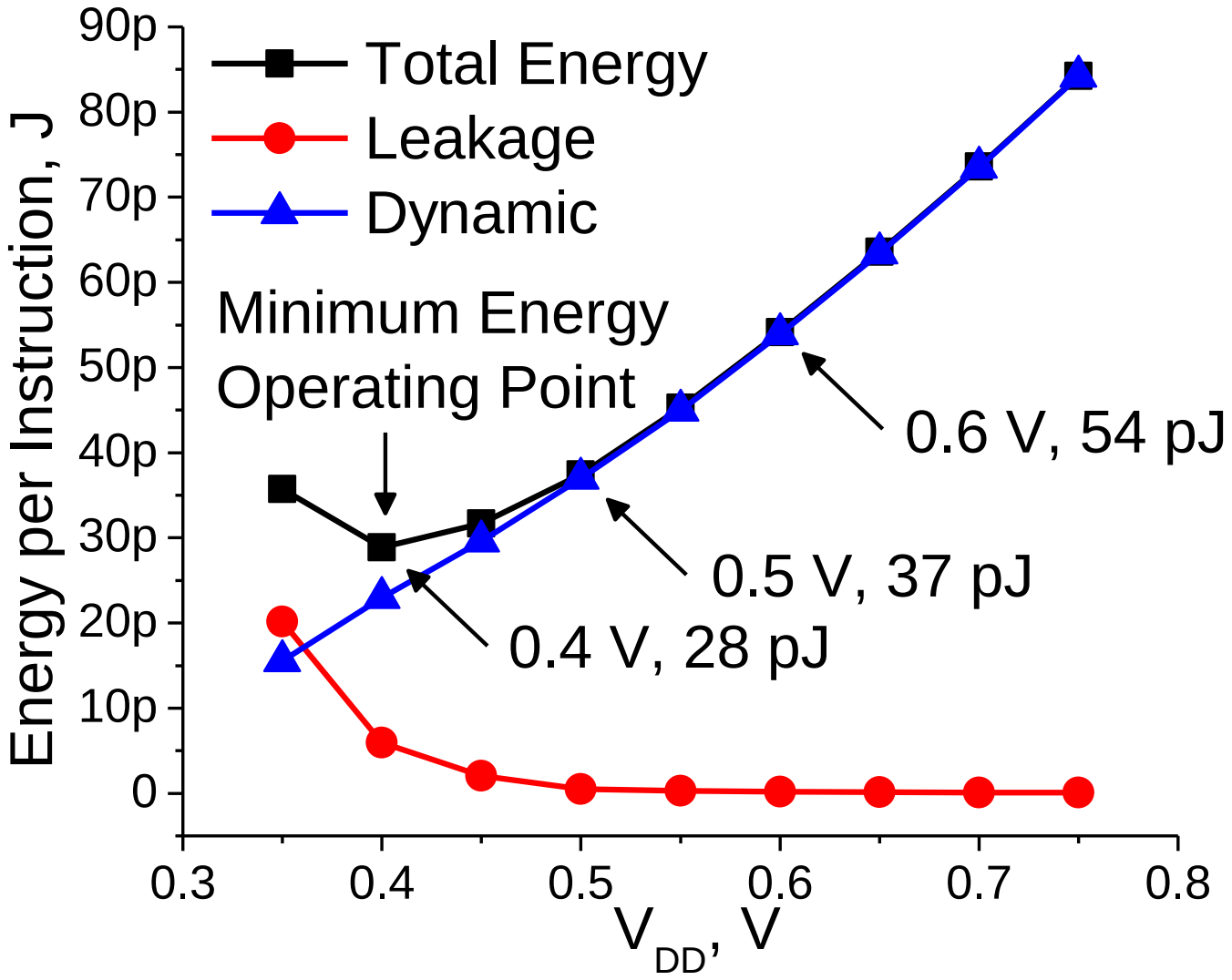
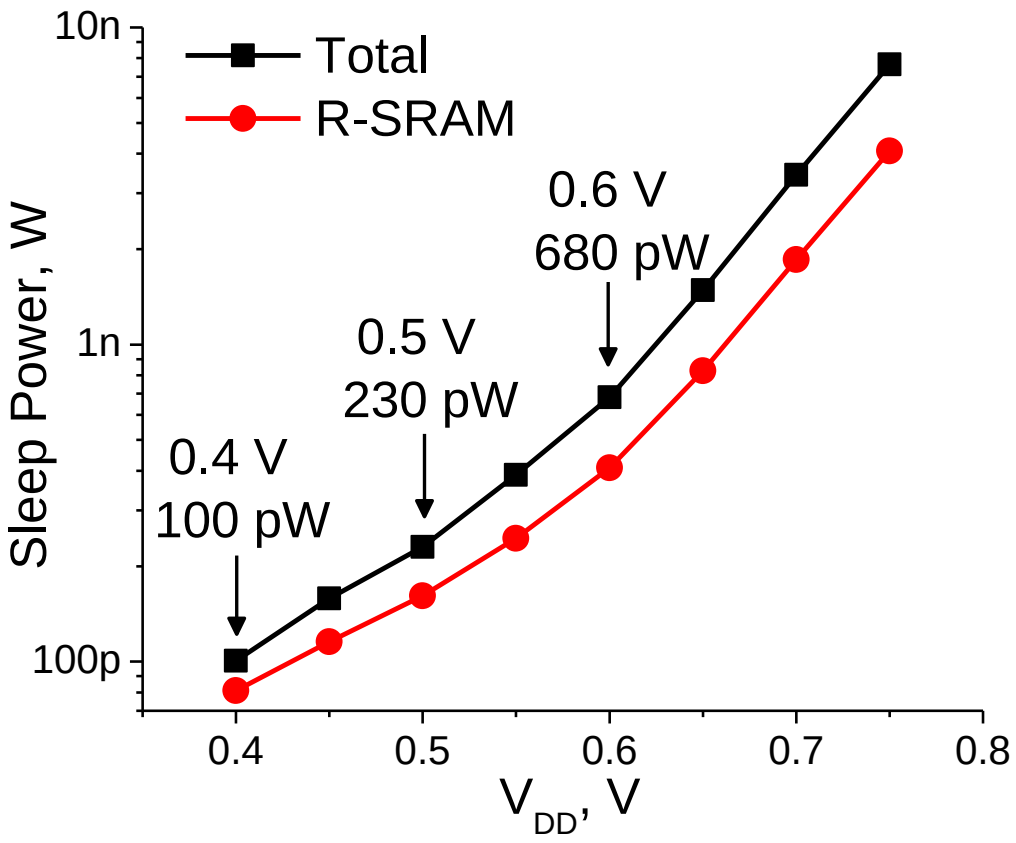


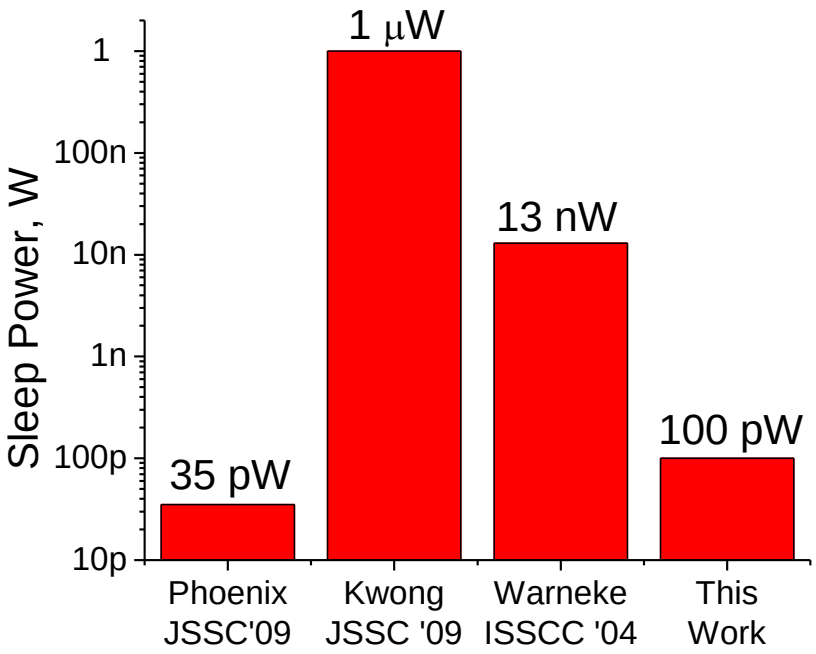
Energy Supplied by PMU



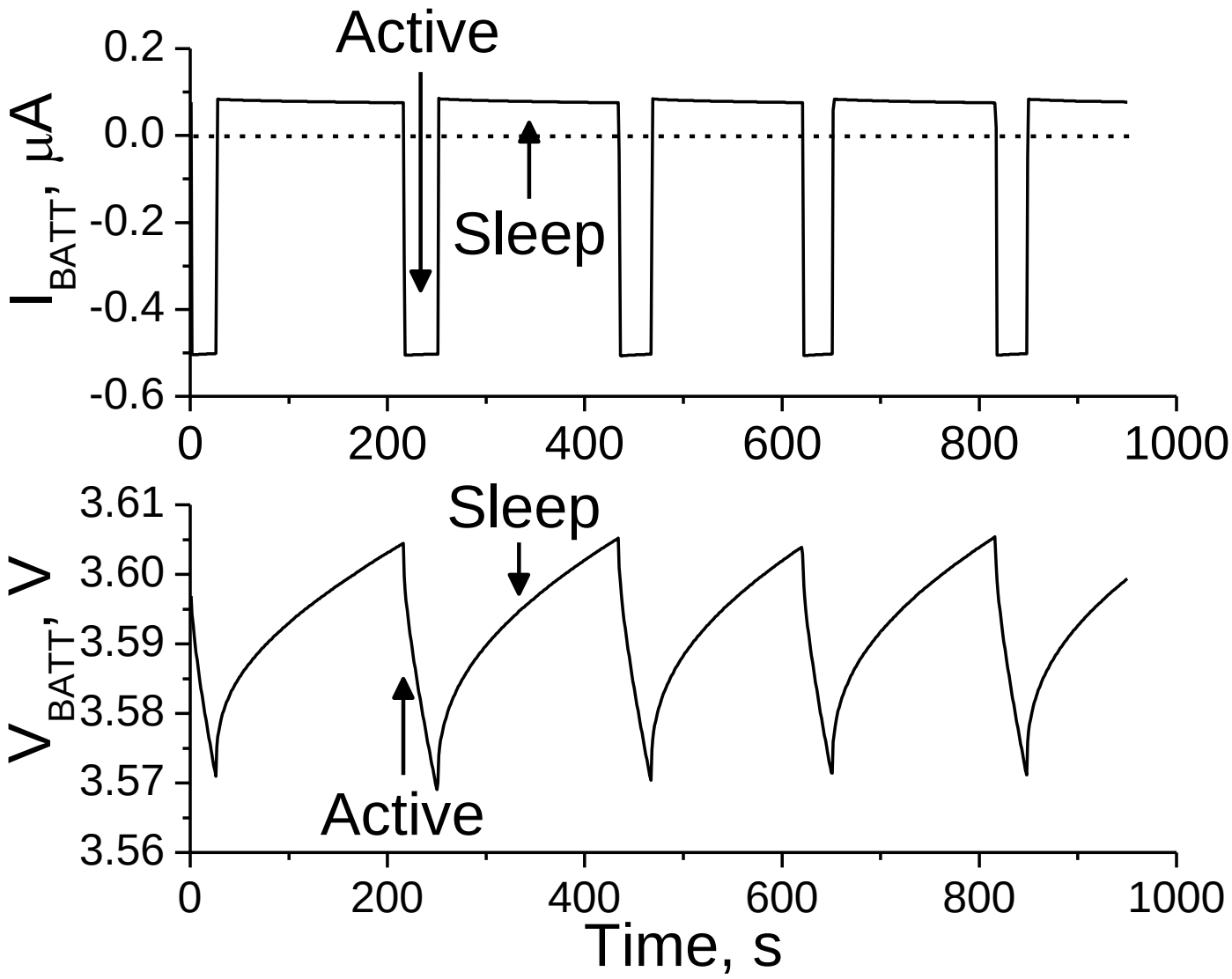
Sleep Power Supplied by PMU



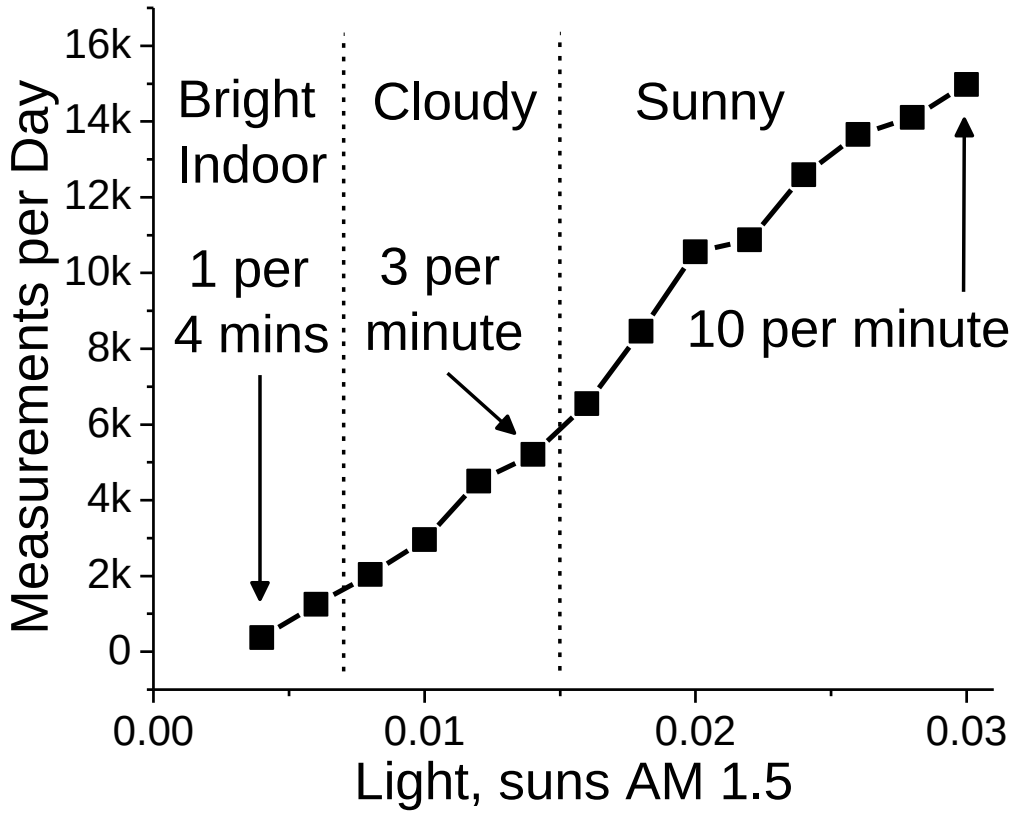
Sleep Power at 400mV	
R-SRAM	80.53%
Timer	19.46%
Cortex-M3	< 0.01%
NR-SRAM	< 0.01%



Nearly-Perpetual Operation



Nearly-Perpetual Usage Model



1 measurement requires 10k instructions

Mode	Harvesting	Lifetime
One measurement every hour	No	5 years
Idle lifetime	No	49 years
Up to10 measurements per minute	Yes	Nearly-infinite

Summary

- Small sensors and long lifetimes create new applications in medical, infrastructure and environmental monitoring
- Size constrains on-sensor energy storage and average power for desired lifetime
- Multi-year lifetime requires sub-nanowatt power consumption
  - Near-threshold processing
  - Low-leakage SRAM
  - Sleep mode power management
- Energy harvesting enables nearly-perpetual operation

Thank You